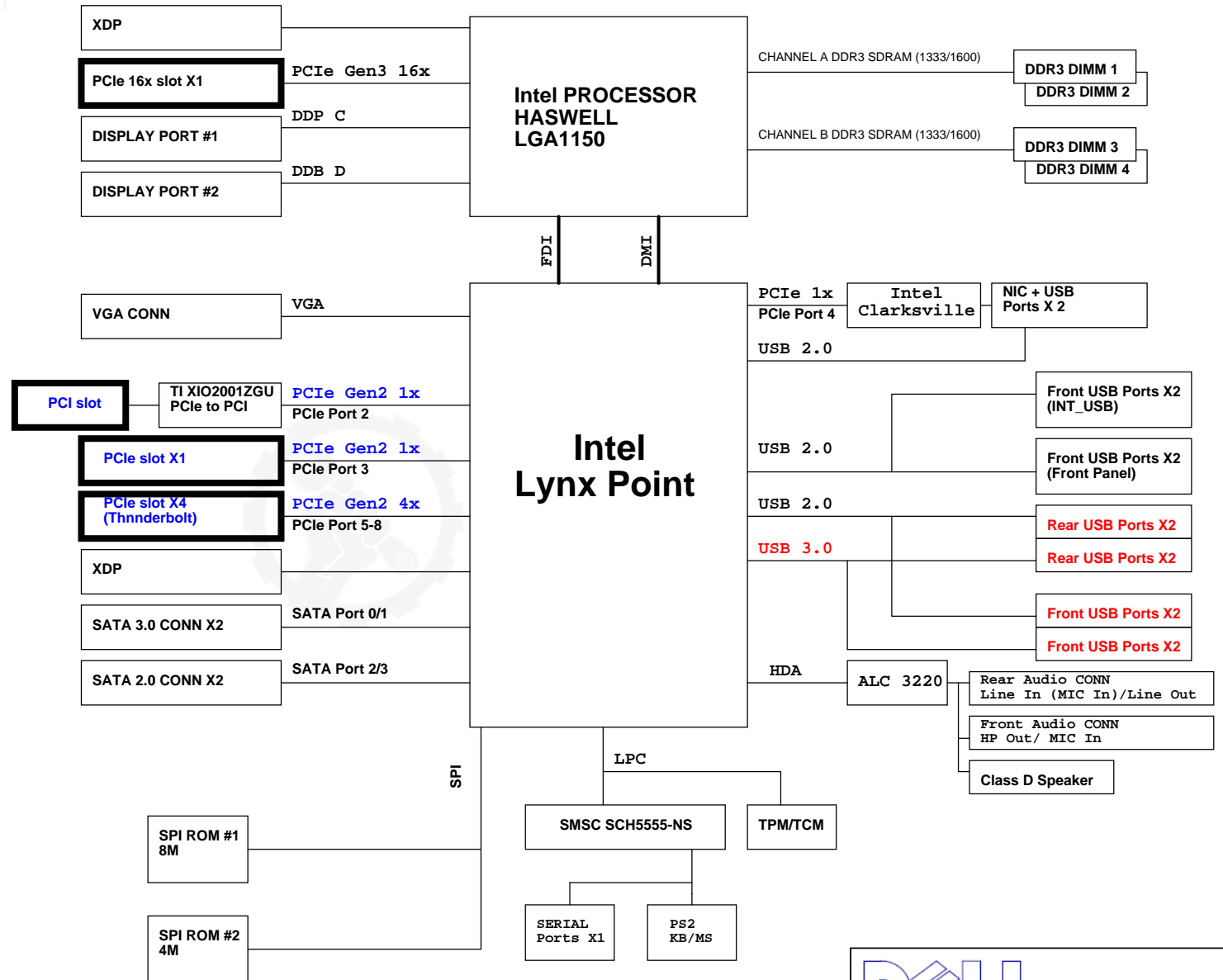



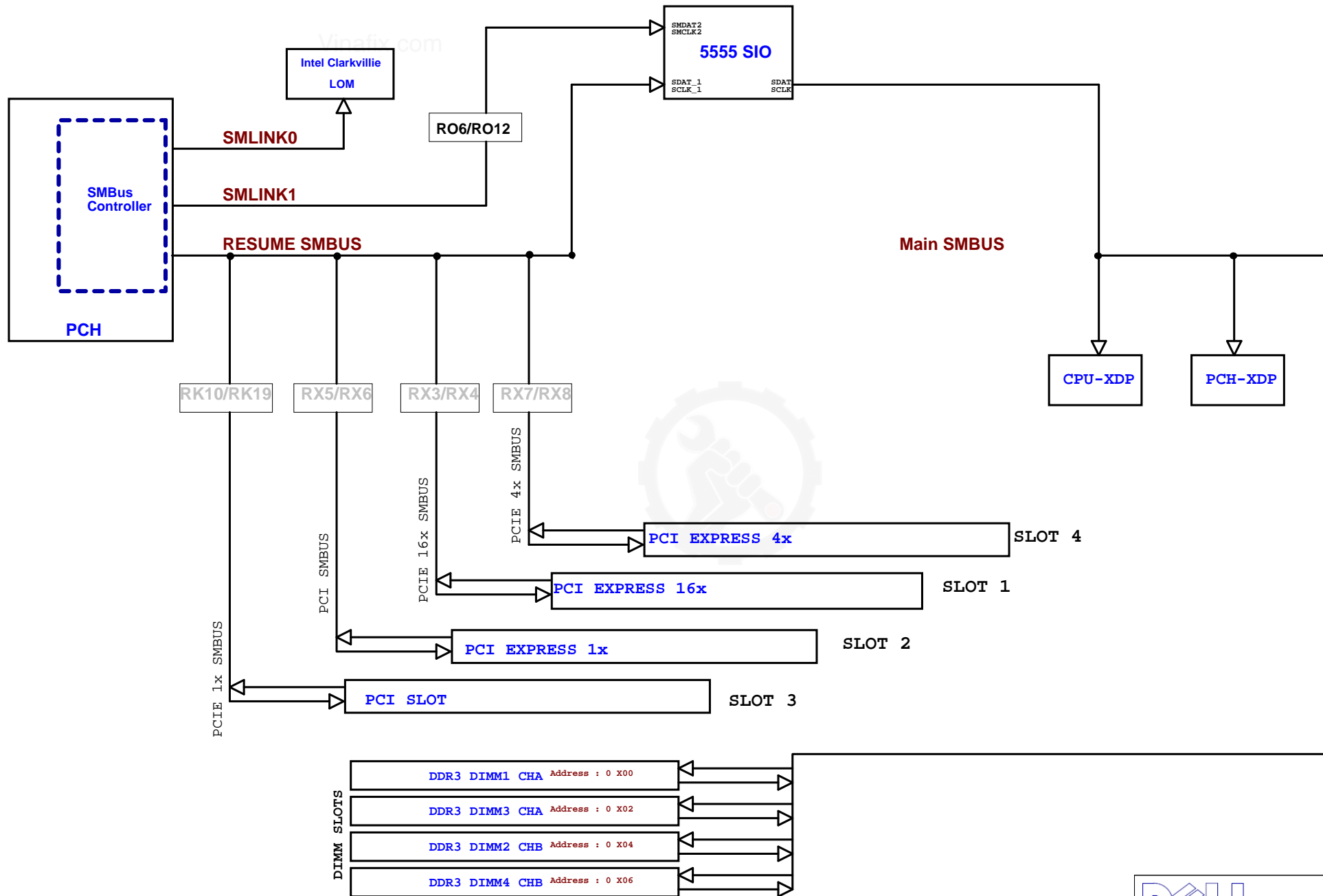
# Tulum/Amazon MT

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<b>Index / Block diagram</b>		
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## SMBUS DIAGRAM



<b>Title</b>
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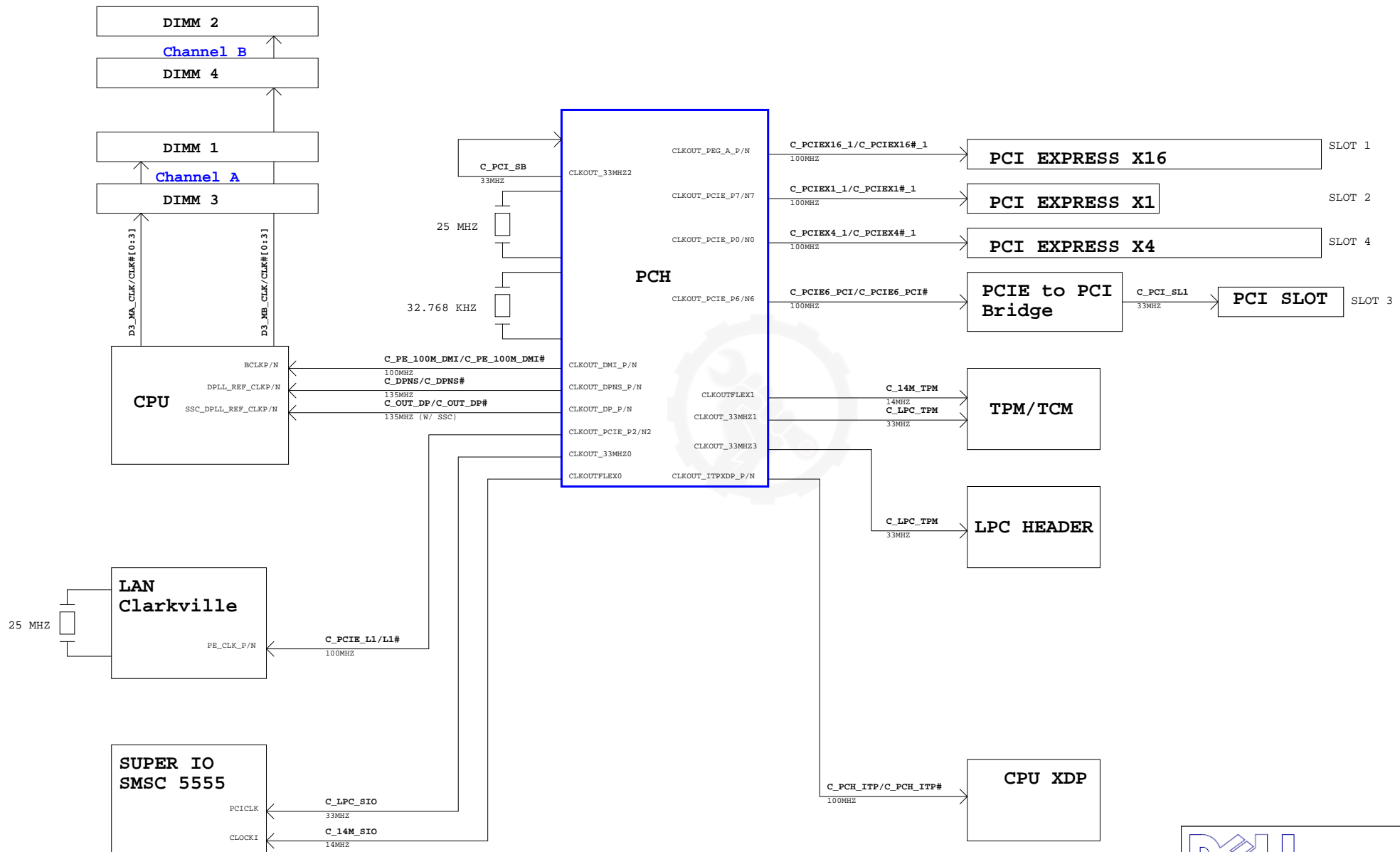
### BLOCK DIAGRAM

DWG NO	
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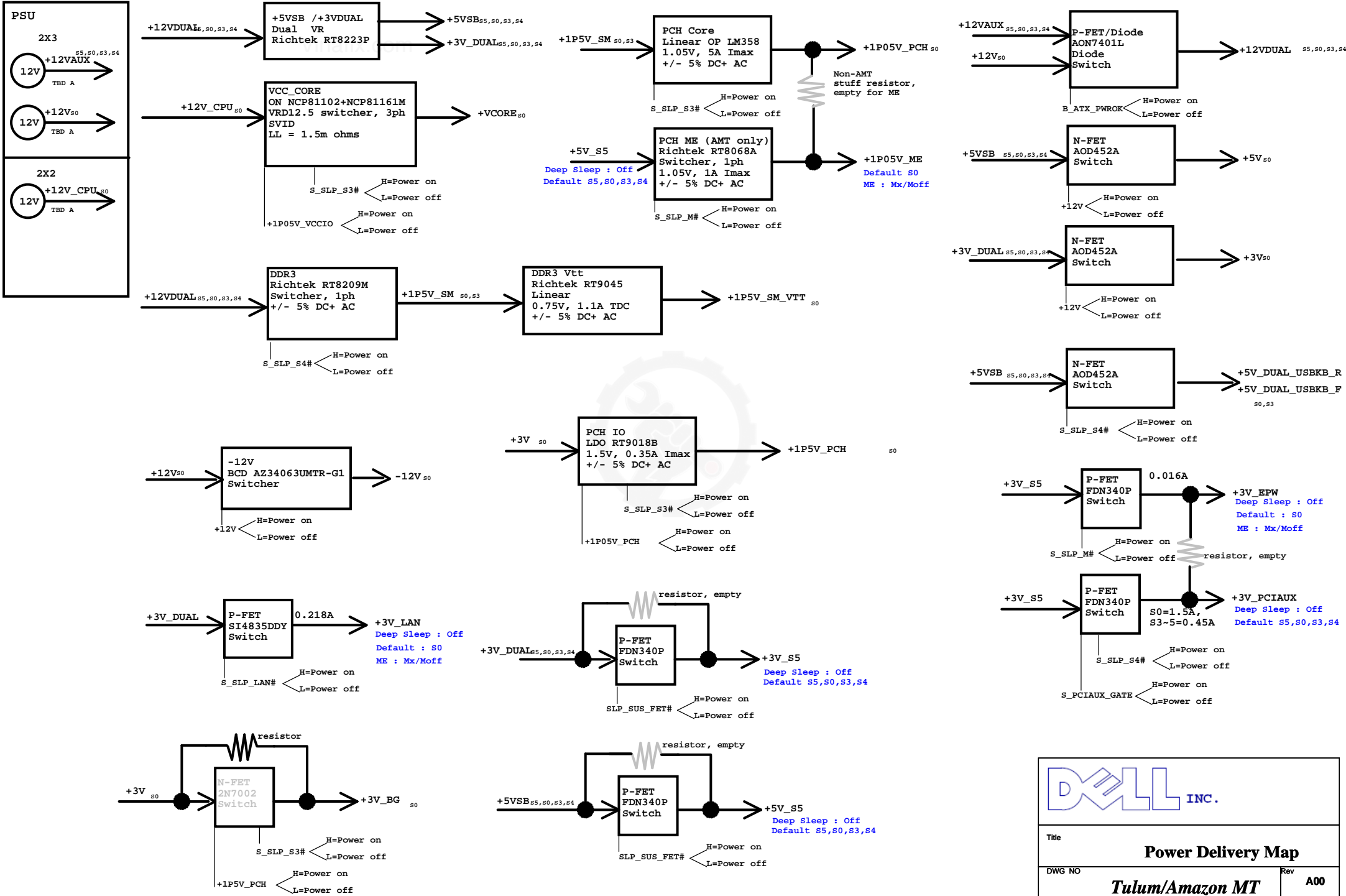
***Tulum/Amazon MT***

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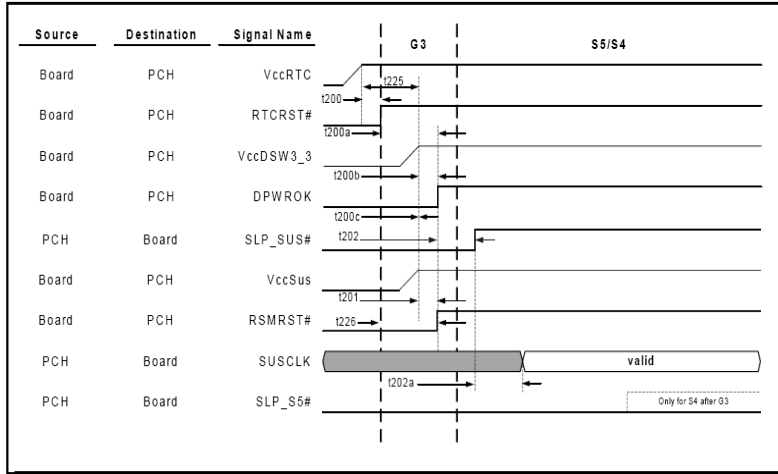
POWER DELIVERY MAP



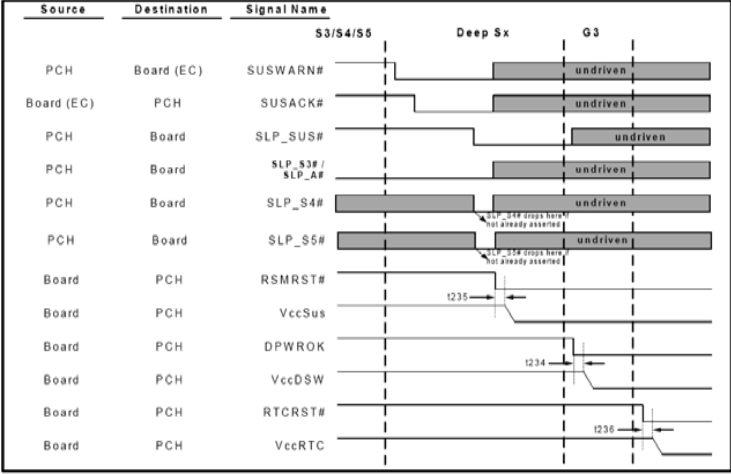
Title		
Power Delivery Map		
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POWER ON Timing Diagram

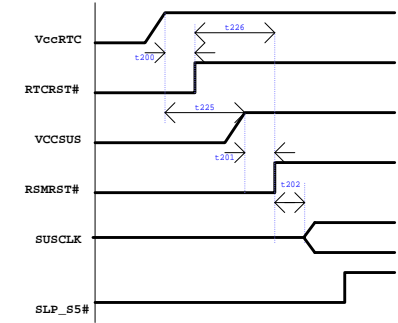
G3 --> S4/S5 (with Deep Sleep support)



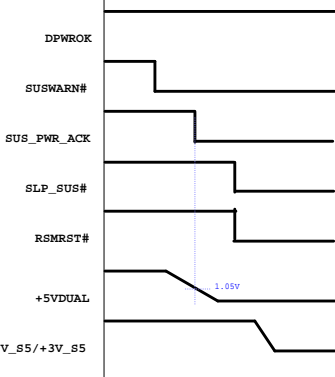
Sx --> Deep S4/S5 -->G3



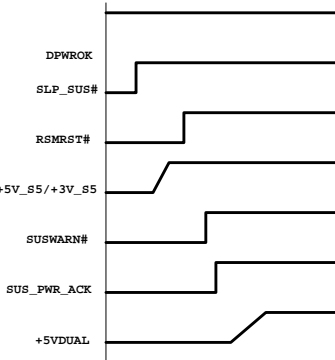
G3 to S4/S5 Timing Diagram



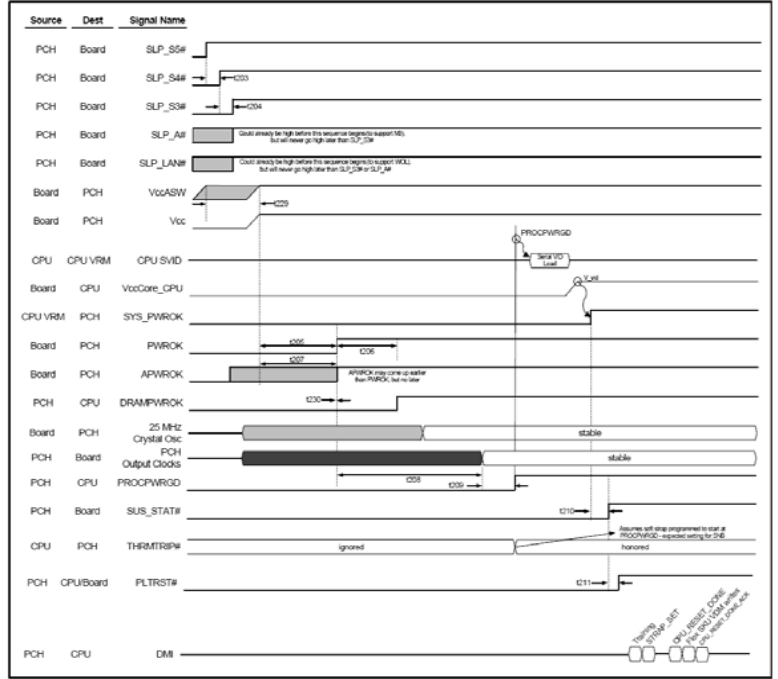
Deep Sleep Entry



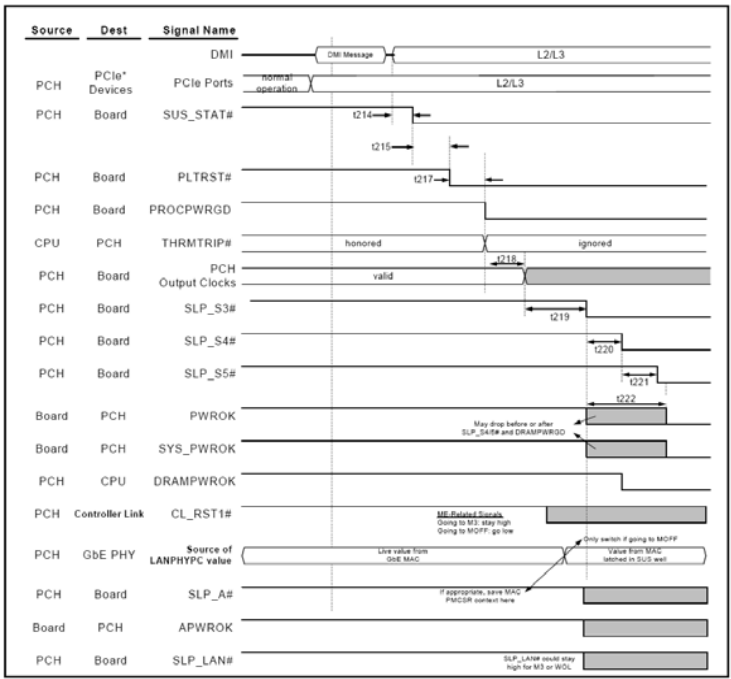
Deep Sleep Exit



S5 --> S0



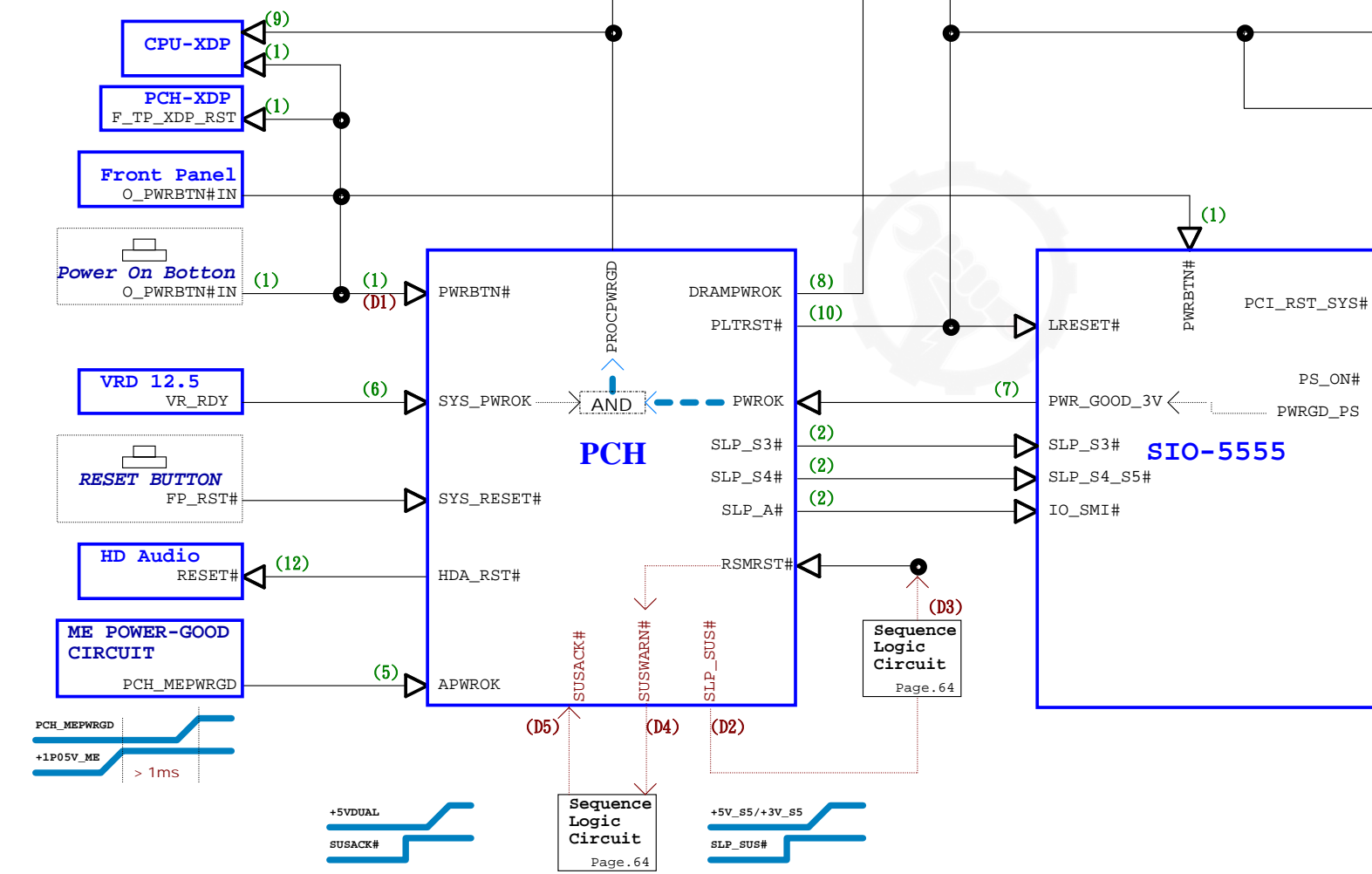
S0 --> S5



RESET / Power Good MAP

Sequence Signal Name:

- (1) O\_PWRBTN#IN
- (2) S\_SLP\_S4# S\_SLP\_S3# S\_SLP\_M#
- (3) O\_PSON#
- (4) B\_ATX\_PWROK
- (5) PCH\_MEPWRGD
- (6) S\_PCH\_SYSPWROK P\_VR\_READY
- (7) PWRGD\_3V
- (8) H\_DRAMPWROK D3\_RESET#
- (9) H\_PWRGD
- (10) S\_PLTRST# H\_RESET#\_R S\_PLTRST#\_R
- (11) X\_PLTRST\_PCIE\_SLOT# K\_PCIRST#\_SLOT
- (12) A\_Z\_RST#



Deep Sleep Exit MAP

Sequence Signal Name:

- (D1) O\_PWRBTN#IN
- (D2) S\_SLP\_SUS#
- (D3) S\_RSMRST#
- (D4) S\_SUSWARN#
- (D5) S\_SUS\_PWR\_ACK#

IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot3	C	D	A	B	18	0	0

STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal <b>Default</b> 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express <b>Default</b>

SIO SMSC5555

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable <b>DEFAULT</b>
DTR1# [TEST_EN] / GP051 (PIN104)	O_DTR1#_R	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI <b>DEFAULT</b>

PCH

On-Die PLL Voltage Regulator Voltage Select

HDA_SYNC	Description	
High	1.5V	<b>DEFAULT</b>
Low	1.8V	

On-Die PLL Voltage Regulator

GPIO28 (IN-PU)	Description	
High	Regulator is enabled.	<b>DEFAULT</b>
Low	Regulator is disabled.	

Topblock Swap Mode

GNT3#/GPIO55 (IN-PU)	Description	
High	Topblock swap mode: Disable	<b>DEFAULT</b>
Low	Topblock swap mode: Enable	

No Reboot Mode

SPER (IN-PD)	Description	
High	No reboot mode: Enable	<b>DEFAULT</b>
Low	No reboot mode: Disable	

Integrated 1.05V VRM

INTVRMEN	Description	
High	Integrated 1.05V VRM: Enable	<b>DEFAULT</b>
Low	Integrated 1.05V VRM: Disable	

TLS Confidentiality

GPIO15 (IN-PD)	Description	
High	ME Crypto TLS cipher suite with confidentiality	<b>DEFAULT</b>
Low	ME Crypto TLS cipher suite with no confidentiality	

Flash Descriptor Override Strap

HDA_SDO	Description	
High	Flash descriptor security will be override	<b>DEFAULT</b>
Low	Disable ME in Manufacturing Mode	

DMI Rx Termination Voltage

SPI_MOSI (IN-PD)	Description	
Low	DMI Rx Termination Voltage	<b>DEFAULT</b>

DMI Termination Voltage

NV_CLE (IN-PU)	Description	
High	DMI and FDI Tx/Rx Termination Voltage	<b>DEFAULT</b>

Boot BIOS Destination Selection

GNT1# (IN-PU)	SATA1GP/GP19 (IN-PU)	Description	
Low	Low	Flash cycle routed to LPC	<b>DEFAULT</b>
High	Low	Flash cycle routed to PCI	
Low	High	Flash cycle routed to NAND	
High	High	Flash cycle routed to SPI	

Deep S4/S5 Well on-die Voltage Regulator Enable

DSWVRMEN	Description	
High	Enable	<b>DEFAULT</b>
Low	Disable	

Digital Port C Strap

DDPC_CTRLDATA	Description	
High	Configure Port C	<b>DEFAULT</b>
Low	Disable	



PCH GPIO Summary				Default	Signal Name	IN-PU/PO	EX-PU/PO	*Current Usage (VDDA/VDDIO/VDDIO2)	
GPIO	Type	Power Well	GPIO						
GPIO00	IO	Core	GPIO	S_GPIO00	—	10k pull-up to +3V	—	E	
GPIO01	IO	Core	GPIO	S_GPIO01	20k IN-PU (only on TACH2)	10k pull-up to +3V 10k pull-down to GND (dummy)	—	E	
GPIO02	IO	Core	GPIO	S_GPIO02	—	8.2k pull-up to +3V	—	NU	
GPIO03	IO	Core	GPIO	S_GPIO03	—	—	—	E	
GPIO04	IO	Core	GPIO	S_GPIO04	—	8.2k pull-up to +3V	—	E	
GPIO05	IO	Core	GPIO	S_GPIO05	—	8.2k pull-up to +3V	—	NU	
GPIO06	IO	Core	GPIO	S_GPIO06	20k IN-PU (only on TACH2)	10k pull-up to +3V	—	NU	
GPIO07	IO	Core	GPIO	S_GPIO07	20k IN-PU (only on TACH2)	10k pull-up to +3V (dummy) 22k pull-down to GND	—	E	
GPIO08	IO	Suspend	GPIO	S_GPIO08	20k IN-PU	—	—	NU	(connected to XDP_PCH)
GPIO09	IO	Suspend	Native	S_GPIO09	—	—	—	Native	
GPIO10	IO	Suspend	Native	S_GPIO10	—	—	—	Native	
GPIO11	IO	Suspend	Native	S_GPIO11	—	10k pull-up to +3V_S5	—	E	
GPIO12	IO	Suspend	Native	S_GPIO12	—	10k pull-up to +3V_LAN 10k pull-down to GND (dummy)	—	O	
GPIO13	IO	Suspend	GPIO	S_GPIO13	—	10k pull-up to +3V_S5	—	NU	
GPIO14	IO	Suspend	GPIO	S_GPIO14	—	10k pull-up to +3V_S5	—	NU	
GPIO15	IO	Suspend	GPIO	S_GPIO15	—	10k pull-up to +3V 10k pull-down to GND (dummy)	—	Strapping	
GPIO16	IO	Core	GPIO	S_GPIO16	20k IN-PU (only on TACH2)	10k pull-up to +3V (dummy) 1k pull-down to GND	—	E	
GPIO17	IO	Core	GPIO	S_GPIO17	—	10k pull-up to +3V	—	E	
GPIO18	IO	Core	GPIO	S_GPIO18	—	10k pull-up to +3V	—	NU	
GPIO19	IO	Core	GPIO	S_GPIO19	20k IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	—	Strapping	
GPIO20	IO	Core	GPIO	S_GPIO20	—	10k pull-up to +3V	—	NU	
GPIO21	IO	Core	GPIO	S_GPIO21	20k IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	—	Strapping	
GPIO22	IO	Core	GPIO	S_GPIO22	—	10k pull-up to +3V	—	NU	
GPIO23	IO	Core	GPIO	S_GPIO23	20k IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	—	Strapping	
GPIO24	IO	Core	GPIO	S_GPIO24	—	10k pull-up to +3V	—	NU	
GPIO25	IO	Core	GPIO	S_GPIO25	20k IN-PU	4.7k pull-down to GND (dummy)	—	Strapping	
GPIO26	IO	Suspend	GPIO	S_GPIO26	—	10k pull-up to +3V_S5	—	NU	
GPIO27	IO	Suspend	Native	S_GPIO27	—	2.2k pull-up to +3V_S5	—	Native	
GPIO28	IO	Suspend	Native	S_GPIO28	—	8.2k pull-up to +3V_S5	—	Native	
GPIO29	IO	Suspend	Native	S_GPIO29	—	10k pull-up to +3V_S5	—	NU	
GPIO30	IO	Suspend	Native	S_GPIO30	—	10k pull-up to +3V_S5	—	NU	
GPIO31	IO	Suspend	Native	S_GPIO31	—	10k pull-up to +3V_S5	—	NU	
GPIO32	IO	Suspend	Native	S_GPIO32	—	10k pull-up to +3V_S5	—	NU	
GPIO33	IO	Suspend	Native	S_GPIO33	—	10k pull-up to +3V_S5	—	NU	
GPIO34	IO	Suspend	Native	S_GPIO34	—	10k pull-up to +3V_S5	—	NU	
GPIO35	IO	Suspend	Native	S_GPIO35	—	10k pull-up to +3V_S5	—	NU	
GPIO36	IO	Suspend	Native	S_GPIO36	—	10k pull-up to +3V_S5	—	NU	
GPIO37	IO	Suspend	Native	S_GPIO37	—	10k pull-up to +3V_S5	—	NU	
GPIO38	IO	Suspend	Native	S_GPIO38	—	10k pull-up to +3V_S5	—	NU	
GPIO39	IO	Suspend	Native	S_GPIO39	—	10k pull-up to +3V_S5	—	NU	
GPIO40	IO	Suspend	Native	S_GPIO40	—	10k pull-up to +3V_S5	—	NU	
GPIO41	IO	Suspend	Native	S_GPIO41	—	10k pull-up to +3V_S5	—	NU	
GPIO42	IO	Suspend	Native	S_GPIO42	—	10k pull-up to +3V_S5	—	NU	
GPIO43	IO	Suspend	Native	S_GPIO43	—	10k pull-up to +3V_S5	—	NU	
GPIO44	IO	Suspend	Native	S_GPIO44	—	10k pull-up to +3V_S5	—	NU	
GPIO45	IO	Suspend	Native	S_GPIO45	—	10k pull-up to +3V_S5	—	NU	
GPIO46	IO	Suspend	Native	S_GPIO46	—	10k pull-up to +3V_S5	—	NU	
GPIO47	IO	Suspend	Native	S_GPIO47	—	10k pull-up to +3V_S5	—	NU	
GPIO48	IO	Suspend	Native	S_GPIO48	—	10k pull-up to +3V_S5	—	NU	
GPIO49	IO	Suspend	Native	S_GPIO49	—	10k pull-up to +3V_S5	—	NU	
GPIO50	IO	Suspend	Native	S_GPIO50	—	10k pull-up to +3V_S5	—	NU	
GPIO51	IO	Suspend	Native	S_GPIO51	—	10k pull-up to +3V_S5	—	NU	
GPIO52	IO	Suspend	Native	S_GPIO52	—	10k pull-up to +3V_S5	—	NU	
GPIO53	IO	Suspend	Native	S_GPIO53	—	10k pull-up to +3V_S5	—	NU	
GPIO54	IO	Suspend	Native	S_GPIO54	—	10k pull-up to +3V_S5	—	NU	
GPIO55	IO	Suspend	Native	S_GPIO55	—	10k pull-up to +3V_S5	—	NU	
GPIO56	IO	Suspend	Native	S_GPIO56	—	10k pull-up to +3V_S5	—	NU	
GPIO57	IO	Suspend	Native	S_GPIO57	—	10k pull-up to +3V_S5	—	NU	
GPIO58	IO	Suspend	Native	S_GPIO58	—	10k pull-up to +3V_S5	—	NU	
GPIO59	IO	Suspend	Native	S_GPIO59	—	10k pull-up to +3V_S5	—	NU	
GPIO60	IO	Suspend	Native	S_GPIO60	—	10k pull-up to +3V_S5	—	NU	
GPIO61	IO	Suspend	Native	S_GPIO61	—	10k pull-up to +3V_S5	—	NU	
GPIO62	IO	Suspend	Native	S_GPIO62	—	10k pull-up to +3V_S5	—	NU	
GPIO63	IO	Suspend	Native	S_GPIO63	—	10k pull-up to +3V_S5	—	NU	
GPIO64	IO	Suspend	Native	S_GPIO64	—	10k pull-up to +3V_S5	—	NU	
GPIO65	IO	Suspend	Native	S_GPIO65	—	10k pull-up to +3V_S5	—	NU	
GPIO66	IO	Suspend	Native	S_GPIO66	—	10k pull-up to +3V_S5	—	NU	
GPIO67	IO	Suspend	Native	S_GPIO67	—	10k pull-up to +3V_S5	—	NU	
GPIO68	IO	Suspend	Native	S_GPIO68	—	10k pull-up to +3V_S5	—	NU	
GPIO69	IO	Suspend	Native	S_GPIO69	—	10k pull-up to +3V_S5	—	NU	
GPIO70	IO	Suspend	Native	S_GPIO70	—	10k pull-up to +3V_S5	—	NU	
GPIO71	IO	Suspend	Native	S_GPIO71	—	10k pull-up to +3V_S5	—	NU	
GPIO72	IO	Suspend	Native	S_GPIO72	—	10k pull-up to +3V_S5	—	NU	
GPIO73	IO	Suspend	Native	S_GPIO73	—	10k pull-up to +3V_S5	—	NU	
GPIO74	IO	Suspend	Native	S_GPIO74	—	10k pull-up to +3V_S5	—	NU	
GPIO75	IO	Suspend	Native	S_GPIO75	—	10k pull-up to +3V_S5	—	NU	

GPIO	Type	Power Well	GPIO	Signal Name	IN-PU/PO	EX-PU/PO	*Current Usage (VDDA/VDDIO/VDDIO2)
GPIO37	IO	Core	GPIO	S_GPIO37	20k IN-PU	1k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO38	IO	Core	GPIO	S_GPIO38	—	10k pull-up to +3V 10k pull-down to GND (dummy)	I
GPIO39	IO	Core	GPIO	S_GPIO39	—	10k pull-up to +3V	I
GPIO40	IO	Suspend	Native	S_GPIO40	—	—	Native
GPIO41	IO	Suspend	Native	S_GPIO41	—	—	Native
GPIO42	IO	Suspend	Native	S_GPIO42	—	—	Native
GPIO43	IO	Suspend	Native	S_GPIO43	—	—	Native
GPIO44	IO	Suspend	Native	S_GPIO44	20k IN-PU	10k pull-up to +3V_S5	I
GPIO45	IO	Suspend	Native	S_GPIO45	—	10k pull-up to +3V_S5	NU
GPIO46	IO	Suspend	Native	S_GPIO46	20k IN-PU	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	I
GPIO47	IO	Core	GPIO	S_GPIO47	—	10k pull-up to +3V (dummy)	I
GPIO48	IO	Core	GPIO	S_GPIO48	—	10k pull-up to +3V	NU
GPIO49	IO	Core	GPIO	S_GPIO49	20k IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO50	IO	Core	GPIO	S_GPIO50	20k IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO51	IO	Core	GPIO	S_GPIO51	—	10k pull-up to +3V	NU
GPIO52	IO	Core	GPIO	S_GPIO52	20k IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO53	IO	Core	GPIO	S_GPIO53	—	10k pull-up to +3V	NU
GPIO54	IO	Core	GPIO	S_GPIO54	—	10k pull-up to +3V	NU
GPIO55	IO	Core	GPIO	S_GPIO55	20k IN-PU	4.7k pull-down to GND (dummy)	Strapping
GPIO56	IO	Suspend	GPIO	S_GPIO56	—	10k pull-up to +3V_S5	NU
GPIO57	IO	Suspend	GPIO	S_GPIO57	—	10k pull-up to +3V_S5	NU
GPIO58	IO	Suspend	Native	S_GPIO58	—	2.2k pull-up to +3V_S5	Native
GPIO59	IO	Suspend	Native	S_GPIO59	—	8.2k pull-up to +3V_S5	Native
GPIO60	IO	Suspend	Native	S_GPIO60	—	10k pull-up to +3V_S5	NU
GPIO61	IO	Suspend	Native	S_GPIO61	—	10k pull-up to +3V_S5 (dummy)	NU
GPIO62	IO	Suspend	Native	S_GPIO62	PU	—	Native
GPIO63	IO	Suspend	Native	S_GPIO63	—	—	Native
GPIO64	IO	Core	Native	S_GPIO64	20k IN-PU	—	NU
GPIO65	IO	Core	Native	S_GPIO65	20k IN-PU	—	Native
GPIO66	IO	Core	Native	S_GPIO66	20k IN-PU	—	NU
GPIO67	IO	Core	Native	S_GPIO67	20k IN-PU	—	Native
GPIO68	IO	Core	GPIO	S_GPIO68	20k IN-PU (only on TACH4)	10k pull-up to +3V (dummy) 22k pull-down to GND	I
GPIO69	IO	Core	GPIO	S_GPIO69	20k IN-PU (only on TACH5)	8.2k pull-up to +3V	I
GPIO70	IO	Core	Native	S_GPIO70	20k IN-PU (only on TACH5)	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO71	IO	Core	Native	S_GPIO71	20k IN-PU (only on TACH7)	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO72	IO	Suspend	Native	S_GPIO72	—	10k pull-up to +3V_S5	NU
GPIO73	IO	Suspend	Native	S_GPIO73	—	10k pull-up to +3V_S5	I
GPIO74	IO	Suspend	Native	S_GPIO74	—	8.2k pull-up to +3V_S5 33k pull-down to GND (dummy)	O
GPIO75	IO	Suspend	Native	S_GPIO75	PU	2.2k pull-up to +3V_S5	Native

SIO_5555 GPIO Summary						
GPIO	PIN NAME	Power well	Signal Name	EX-PU/ID	*Current Usage (CPU/Flash/Strapping)	Programming Function
GPIO00	GPIO00	V3_S5	NC	NA	Native	NA
GPIO01	GPIO01	V3_S5	NC	NA	Native	NA
GPIO02	GPIO02	V3_S5	NC	NA	Native	NA
GPIO03	GPIO03	V3_S5	NC	NA	Native	NA
GPIO04	SUSWAKE / GPIO04	V3_S5	S_SUSWAKE	NA	Native	NA
GPIO05	H_CPLURSTK / GPIO05 / REQ_REQUEST	V3_S5	O_PECU_REQ	10k pull-up to +3V	Native	NA
GPIO06	YELLOW / GPIO06	V3_S5	O_YELLOW	40k pull-up to +5V_S5	Native	NA
GPIO07	GREEN / GPIO07	V3_S5	O_GREEN	40k pull-up to +5V_S5	Native	NA
GPIO08	SMODAT2 / GPIO08	V3_S5	S_SMLDATA	2.2k pull-up to +3V_S5	Native	NA
GPIO09	SMODAT2 / GPIO09	V3_S5	S_SMLDATA	2.2k pull-up to +3V_S5	Native	NA
GPIO10	SMODAT2 / GPIO10	V3_S5	S_SMLDATA	2.2k pull-up to +3V_S5	Native	NA
GPIO11	SMODAT2 / GPIO11	V3_S5	S_SMLDATA	2.2k pull-up to +3V_S5	Native	NA
GPIO12	SMODAT2 / GPIO12	V3_S5	S_SMLDATA	2.2k pull-up to +3V_S5	Native	NA
GPIO13	SMODAT2 / GPIO13	V3_S5	S_SMLDATA	2.2k pull-up to +3V_S5	Native	NA
GPIO14	TMN_SHIFT / GPIO14	V3_S5	TMN_SHIFT	8.2k pull-up to +3V_S5 33k pull-down to GND (Dummy)	I	1: default 0: TMN shift adjustment
GPIO15	PWRSTW / GPIO15	V3_S5	O_PWRSTW	1k pull-up to +3V_DUAL (Dummy)	Native	NA
GPIO16	PROGSHOT / GPIO16	V3_S5	H_PROGSHOT	510k pull-up to H_CPU_VCCIO_RN	Native	NA
GPIO17	TACH2 / GPIO17	V3_S5	O_TACH2	1k pull-up to +3V	Native	NA
GPIO18	TACH2 / GPIO18	V3_S5	O_TACH2	1k pull-up to +3V	Native	NA
GPIO19	TACH2 / GPIO19	V3_S5	O_TACH2	1k pull-up to +3V	Native	NA
GPIO20	TACH2 / GPIO20	V3_S5	O_TACH2	1k pull-up to +3V	Native	NA
GPIO21	PWM1 / GPIO21	V3_S5	O_PUFAN_PWM	4.7k pull-up to +3V	Native	NA
GPIO22	PWM1 / GPIO22	V3_S5	O_PUFAN_PWM	4.7k pull-up to +3V	Native	NA
GPIO23	PWM2 / GPIO23	V3_S5	O_CHAFAN_PWM	4.7k pull-up to +3V	Native	NA
GPIO24	PWM3 / GPIO24	V3_S5	NC	NA	Native	NA
GPIO25	FP_CBL_DET / GPIO25	V3_S5	O_FP_CBL_DET	8.2k pull-up to +3V_S5	I	1: default 0: power switch cable plugged
GPIO26	POL_RST_5V5 / GPIO26	V3_S5	X_PLTRST_POL_RST	NA	Native	NA
GPIO27	POL_RST_5V5 / GPIO27	V3_S5	NC	NA	Native	NA
GPIO28	POL_RST_5V5 / GPIO28	V3_S5	NC	NA	Native	NA
GPIO29	POL_RST_5V5 / GPIO29	V3_S5	NC	NA	Native	NA
GPIO30	P5_5V5 / GPIO30	V3_S5	O_P5V5	4.7k pull-up to +5V5	Native	NA
GPIO31	FP_SPEAKER_DET / GPIO31	V3_S5	O_AUDIO_FCSPEAKER_DET	8.2k pull-up to +3V_S5	I	1: default 0: FP speaker cable plugged
GPIO32	SUS3V_FAN / GPIO32	V3_S5	O_SUS3V_FAN	NA	Native	NA
GPIO33	PWR_3000_V / GPIO33	V3_S5	PWR3000_V	NA	Native	NA
GPIO34	RGMRSTW / GPIO34	V3_S5	O_RGMRSTW	NA	Native	NA
GPIO35	LATCHED_BF_OUT / GPIO35	V3_S5	NC	NA	Native	NA
GPIO36	QPS28 / SML_CLK1	V3_S5	NC	NA	Native	NA
GPIO37	QPS40 / SML_DAT1	V3_S5	NC	NA	Native	NA
GPIO38	QPS41 / IO_PMB	V3_S5	O_PMB	10k pull-up to +3V_S5	Native	NA
GPIO39	GPIO39	V3_S5	NC	NA	Native	NA
GPIO40	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO41	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO42	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO43	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO44	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO45	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO46	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO47	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO48	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO49	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO50	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO51	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO52	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO53	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO54	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO55	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO56	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO57	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO58	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO59	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO60	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO61	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO62	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO63	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO64	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO65	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO66	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO67	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO68	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO69	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO70	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO71	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO72	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO73	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO74	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO75	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO76	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO77	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO78	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO79	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO80	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO81	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO82	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO83	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO84	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO85	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO86	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO87	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO88	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO89	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO90	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO91	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO92	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO93	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO94	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO95	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO96	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO97	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO98	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO99	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO100	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO101	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO102	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO103	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO104	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO105	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO106	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO107	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO108	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO109	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO110	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO111	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO112	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO113	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO114	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO115	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO116	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO117	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO118	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO119	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO120	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO121	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO122	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO123	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO124	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO125	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO126	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO127	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO128	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO129	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO130	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO131	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO132	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO133	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO134	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO135	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO136	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO137	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO138	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO139	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO140	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO141	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO142	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO143	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO144	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO145	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO146	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO147	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO148	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO149	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO150	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO151	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO152	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO153	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO154	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO155	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO156	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO157	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO158	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO159	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO160	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO161	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO162	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO163	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO164	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO165	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO166	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO167	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO168	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO169	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO170	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO171	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO172	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO173	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO174	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO175	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO176	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO177	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO178	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO179	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO180	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO181	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO182	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO183	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO184	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO185	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO186	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO187	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO188	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO189	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO190	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO191	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO192	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO193	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	NA
GPIO194	QPS41 / QPS40	V3_S5	O_QPS41_R	NA	Native	



# DDR3 CH-A

[15,16] D3\_DQ\_A[63..0] <<>

D3\_MAA[15..0] [15,16]

ECC

D3\_CKE\_A0 [15]  
D3\_CKE\_A1 [15]  
D3\_CKE\_A2 [16]  
D3\_CKE\_A3 [16]

D3\_SCS\_A#0 [15]  
D3\_SCS\_A#1 [15]  
D3\_SCS\_A#2 [16]  
D3\_SCS\_A#3 [16]

D3\_MA\_CLK0 [15]  
D3\_MA\_CLK#0 [15]  
D3\_MA\_CLK1 [15]  
D3\_MA\_CLK#1 [15]  
D3\_MA\_CLK2 [16]  
D3\_MA\_CLK#2 [16]  
D3\_MA\_CLK3 [16]  
D3\_MA\_CLK#3 [16]

D3\_RASA# [15,16]  
D3\_WEA# [15,16]

D3\_CASA# [15,16]  
D3\_RESET# [15,16,17,18]

BIT SWIZZLE TABLE

DDR0_DQ[8]	AH40	DQ 9
DDR0_DQ[9]	AH39	DQ 13
DDR0_DQ[13]	AH38	DQ 8
DDR0_DQ[16]	AM40	DQ 17
DDR0_DQ[17]	AM39	DQ 21
DDR0_DQ[21]	AM38	DQ 16
DDR0_DQ[24]	AV37	DQ 25
DDR0_DQ[25]	AW37	DQ 29
DDR0_DQ[29]	AU37	DQ 24
DDR0_DQ[32]	AY6	DQ 33
DDR0_DQ[33]	AU6	DQ 37
DDR0_DQ[37]	AV6	DQ 32
DDR0_DQ[40]	AR1	DQ 41
DDR0_DQ[41]	AR4	DQ 45
DDR0_DQ[45]	AR3	DQ 40
DDR0_DQ[48]	AL1	DQ 49
DDR0_DQ[49]	AL4	DQ 53
DDR0_DQ[53]	AL3	DQ 48
DDR0_DQ[56]	AG1	DQ 57
DDR0_DQ[57]	AG4	DQ 61
DDR0_DQ[61]	AG3	DQ 56
DDR0_DQ[64]	AW33	DQ 65
DDR0_DQ[65]	AV33	DQ 69
DDR0_DQ[69]	AU33	DQ 64

Bit Swap for layout

ECC

ECC

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# DDR3 CH-B

[17,18] D3\_DQ\_B[63..0]

Vinafix

D3_DQ_B0	AE34	SB_DQ[0]
D3_DQ_B1	AE35	SB_DQ[1]
D3_DQ_B2	AG35	SB_DQ[2]
D3_DQ_B3	AH35	SB_DQ[3]
D3_DQ_B4	AD34	SB_DQ[4]
D3_DQ_B5	AD35	SB_DQ[5]
D3_DQ_B6	AG34	SB_DQ[6]
D3_DQ_B7	AH34	SB_DQ[7]
D3_DQ_B8	AL34	SB_DQ[8]
D3_DQ_B9	AK35	SB_DQ[9]
D3_DQ_B10	AK31	SB_DQ[10]
D3_DQ_B11	AL31	SB_DQ[11]
D3_DQ_B12	AK34	SB_DQ[12]
D3_DQ_B13	AK35	SB_DQ[13]
D3_DQ_B14	AK32	SB_DQ[14]
D3_DQ_B15	AL32	SB_DQ[15]
D3_DQ_B17	AP34	SB_DQ[16]
D3_DQ_B19	AN31	SB_DQ[17]
D3_DQ_B23	AP31	SB_DQ[18]
D3_DQ_B20	AN35	SB_DQ[19]
D3_DQ_B16	AP35	SB_DQ[20]
D3_DQ_B18	AN32	SB_DQ[21]
D3_DQ_B22	AP32	SB_DQ[22]
D3_DQ_B25	AM29	SB_DQ[23]
D3_DQ_B28	AM28	SB_DQ[24]
D3_DQ_B27	AR29	SB_DQ[25]
D3_DQ_B30	AR28	SB_DQ[26]
D3_DQ_B24	AL29	SB_DQ[27]
D3_DQ_B29	AL28	SB_DQ[28]
D3_DQ_B26	AP29	SB_DQ[29]
D3_DQ_B31	AP28	SB_DQ[30]
D3_DQ_B32	AR12	SB_DQ[31]
D3_DQ_B33	AP12	SB_DQ[32]
D3_DQ_B34	AL13	SB_DQ[33]
D3_DQ_B35	AL12	SB_DQ[34]
D3_DQ_B36	AR13	SB_DQ[35]
D3_DQ_B37	AP13	SB_DQ[36]
D3_DQ_B38	AM13	SB_DQ[37]
D3_DQ_B39	AM12	SB_DQ[38]
D3_DQ_B45	AR9	SB_DQ[39]
D3_DQ_B41	AP9	SB_DQ[40]
D3_DQ_B47	AR6	SB_DQ[41]
D3_DQ_B43	AP6	SB_DQ[42]
D3_DQ_B44	AR10	SB_DQ[43]
D3_DQ_B40	AP10	SB_DQ[44]
D3_DQ_B46	AR7	SB_DQ[45]
D3_DQ_B42	AP7	SB_DQ[46]
D3_DQ_B52	AM9	SB_DQ[47]
D3_DQ_B53	AL9	SB_DQ[48]
D3_DQ_B50	AL6	SB_DQ[49]
D3_DQ_B55	AL7	SB_DQ[50]
D3_DQ_B48	AM10	SB_DQ[51]
D3_DQ_B49	AL10	SB_DQ[52]
D3_DQ_B54	AM6	SB_DQ[53]
D3_DQ_B51	AM7	SB_DQ[54]
D3_DQ_B61	AH6	SB_DQ[55]
D3_DQ_B60	AH7	SB_DQ[56]
D3_DQ_B59	AE6	SB_DQ[57]
D3_DQ_B63	AE7	SB_DQ[58]
D3_DQ_B56	AJ6	SB_DQ[59]
D3_DQ_B57	AJ7	SB_DQ[60]
D3_DQ_B58	AF6	SB_DQ[61]
D3_DQ_B62	AF7	SB_DQ[62]
		SB_DQ[63]
	AF35	SB_DQS[0]
	AL33	SB_DQS[1]
	AP33	SB_DQS[2]
	AN28	SB_DQS[3]
	AN12	SB_DQS[4]
	AP8	SB_DQS[5]
	AL8	SB_DQS[6]
	AG7	SB_DQS[7]
	AN25	SB_DQS[8]
	AF34	SB_DQS[9]
	AK33	SB_DQS[10]
	AN33	SB_DQS[11]
	AN29	SB_DQS[12]
	AN13	SB_DQS[13]
	AR8	SB_DQS[14]
	AM8	SB_DQS[15]
	AG6	SB_DQS[16]
	AN26	SB_DQS[17]
		SB_DQS[18]

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SB_MA[0]	AL19	D3_MAB0
SB_MA[1]	AK23	D3_MAB1
SB_MA[2]	AM22	D3_MAB2
SB_MA[3]	AM23	D3_MAB3
SB_MA[4]	AP23	D3_MAB4
SB_MA[5]	AL23	D3_MAB5
SB_MA[6]	AY24	D3_MAB6
SB_MA[7]	AV25	D3_MAB7
SB_MA[8]	AU26	D3_MAB8
SB_MA[9]	AW25	D3_MAB9
SB_MA[10]	AP18	D3_MAB10
SB_MA[11]	AY25	D3_MAB11
SB_MA[12]	AV26	D3_MAB12
SB_MA[13]	AR15	D3_MAB13
SB_MA[14]	AV27	D3_MAB14
SB_MA[15]	AY28	D3_MAB15

D3\_MAB[15..0] [17,18]

SB_ODT[0]	AM17	D3_ODT_B0 [17]
SB_ODT[1]	AL16	D3_ODT_B1 [17]
SB_ODT[2]	AM16	D3_ODT_B2 [18]
SB_ODT[3]	AK15	D3_ODT_B3 [18]

SB_ECC_CB[0]	AM26	D3_SB_ECC_CB4 [17,18]
SB_ECC_CB[1]	AM25	D3_SB_ECC_CB5 [17,18]
SB_ECC_CB[2]	AP25	D3_SB_ECC_CB6 [17,18]
SB_ECC_CB[3]	AP26	D3_SB_ECC_CB7 [17,18]
SB_ECC_CB[4]	AL26	D3_SB_ECC_CB8 [17,18]
SB_ECC_CB[5]	AL25	D3_SB_ECC_CB9 [17,18]
SB_ECC_CB[6]	AR26	D3_SB_ECC_CB2 [17,18]
SB_ECC_CB[7]	AR25	D3_SB_ECC_CB3 [17,18]

D3\_BAB[2..0] [17,18]

SB_BS[0]	AK17	D3_BAB0
SB_BS[1]	AL18	D3_BAB1
SB_BS[2]	AW28	D3_BAB2

SB_CKE[0]	AW29	D3_CKE_B0 [17]
SB_CKE[1]	AY29	D3_CKE_B1 [17]
SB_CKE[2]	AU28	D3_CKE_B2 [18]
SB_CKE[3]	AU29	D3_CKE_B3 [18]

SB_CS#[0]	AP17	D3_SCS_B#0 [17]
SB_CS#[1]	AN15	D3_SCS_B#1 [17]
SB_CS#[2]	AN17	D3_SCS_B#2 [18]
SB_CS#[3]	AL15	D3_SCS_B#3 [18]

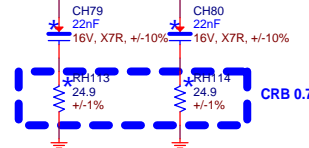
SB_CK[0]	AM20	D3_MB_CLK0 [17]
SB_CK#[0]	AM21	D3_MB_CLK#0 [17]
SB_CK[1]	AP22	D3_MB_CLK1 [17]
SB_CK#[1]	AP21	D3_MB_CLK#1 [17]

SB_CK[2]	AN20	D3_MB_CLK2 [18]
SB_CK#[2]	AN21	D3_MB_CLK#2 [18]
SB_CK[3]	AP19	D3_MB_CLK3 [18]
SB_CK#[3]	AP20	D3_MB_CLK#3 [18]

SB_CAS#	AP16	D3_CASB# [17,18]
RSVD_49	AL20	
SB_RAS#	AM18	D3_RASB# [17,18]
SB_WEB#	AK16	D3_WEB# [17,18]

SA_DIMM_VREFDQ	AB39	H CPU DIMM VREF A
SB_DIMM_VREFDQ	AB40	H CPU DIMM VREF B

H_CPU_DIMM_VREF_A	[15]
H_CPU_DIMM_VREF_B	[17]



CRB 0.7



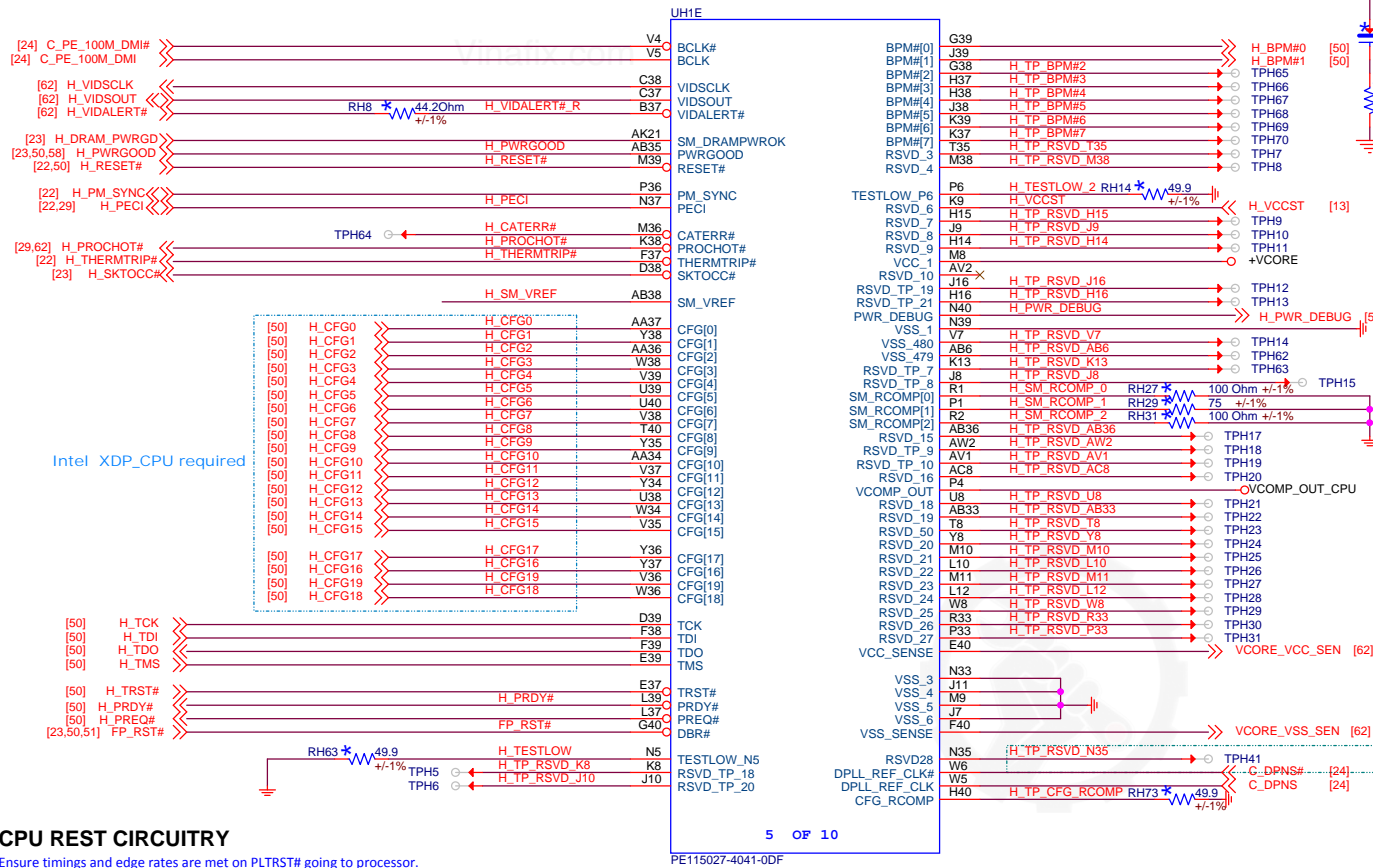
Title  
**CPU-2: DDR3\_CHB**

DWG NO  
**Tulum/Amazon MT**

Date: Tuesday, January 29, 2013 Sheet 10 of 66

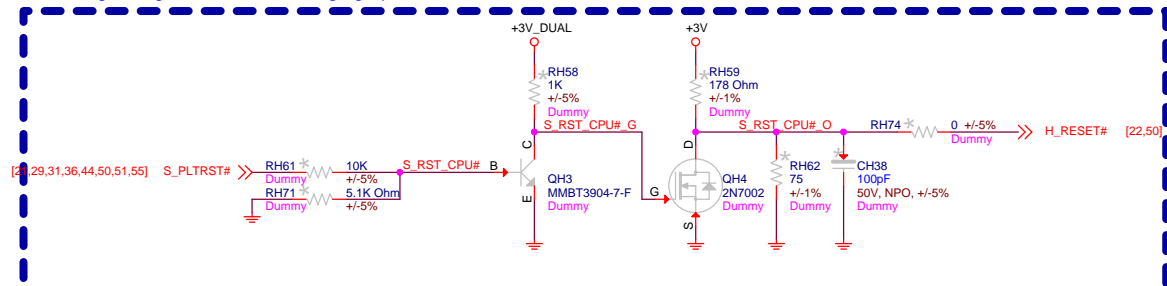
Rev  
**A00**

**MCP - VID,CTRL, MSIC**



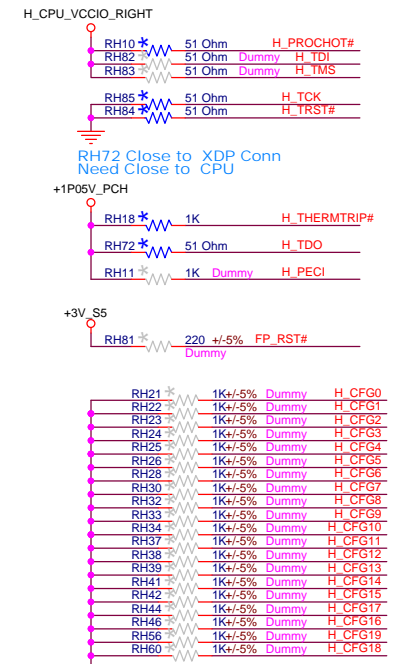
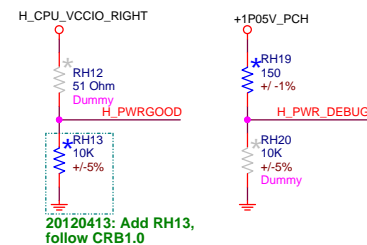
## CPU REST CIRCUITRY

Ensure timings and edge rates are met on PLTRST# going to processor.

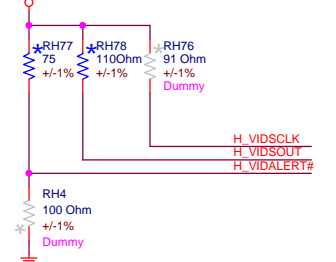


Check with Intel for this circuit necessary ??

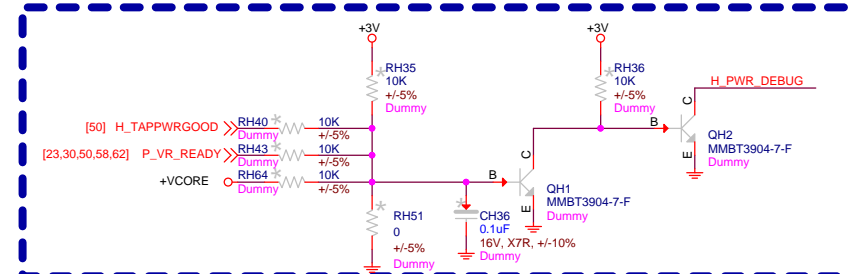
If RS71 pop, CPU RESET CIRCUIT need to Dummy



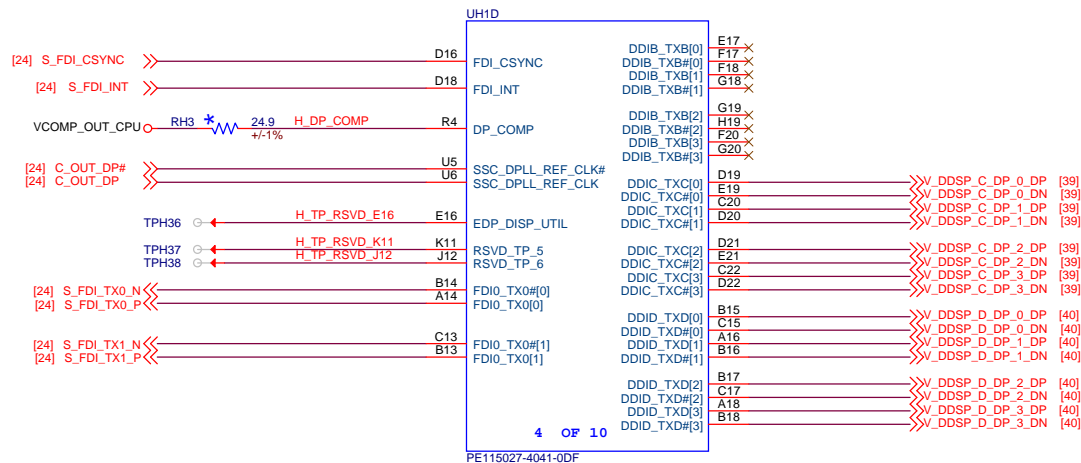
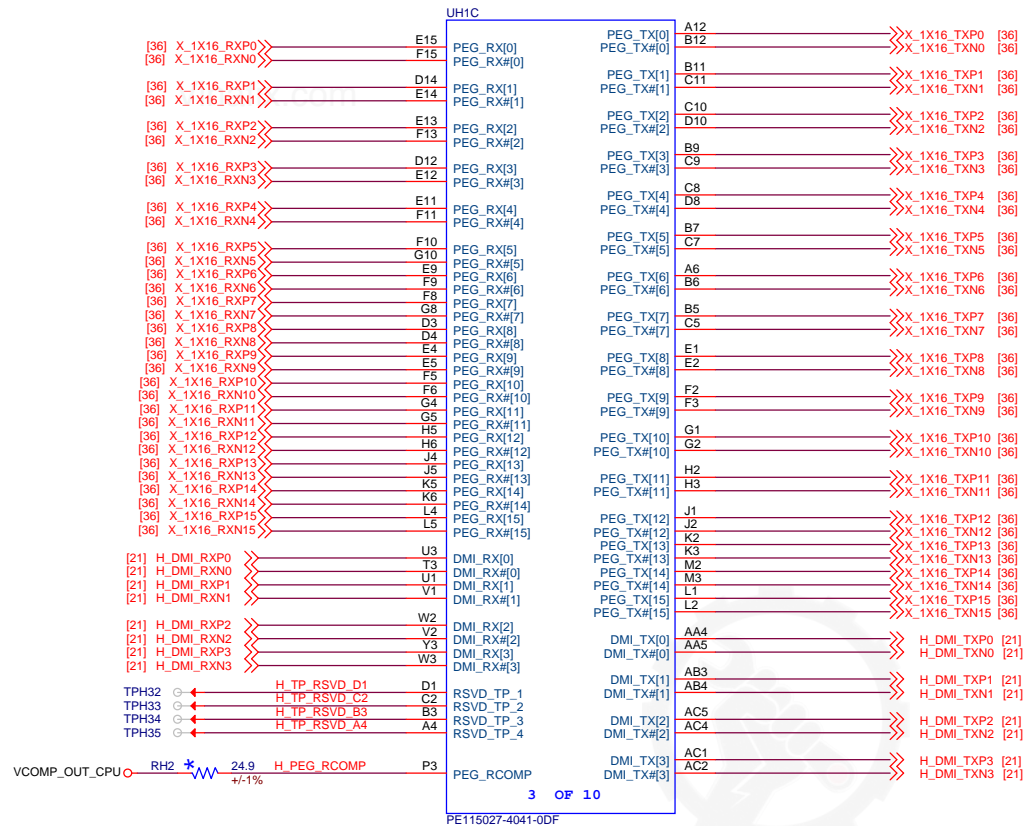
H\_CPU\_VCCIO\_RIGHT



Check with Intel for this circuit necessary ??




Title			
<b>CPU-3: VID/MISC</b>			
DWG NO			Rev
<b><i>Tulum/Amazon MT</i></b>			<b>A00</b>
Date:	Tuesday, January 29, 2013	Sheet	11 of 66

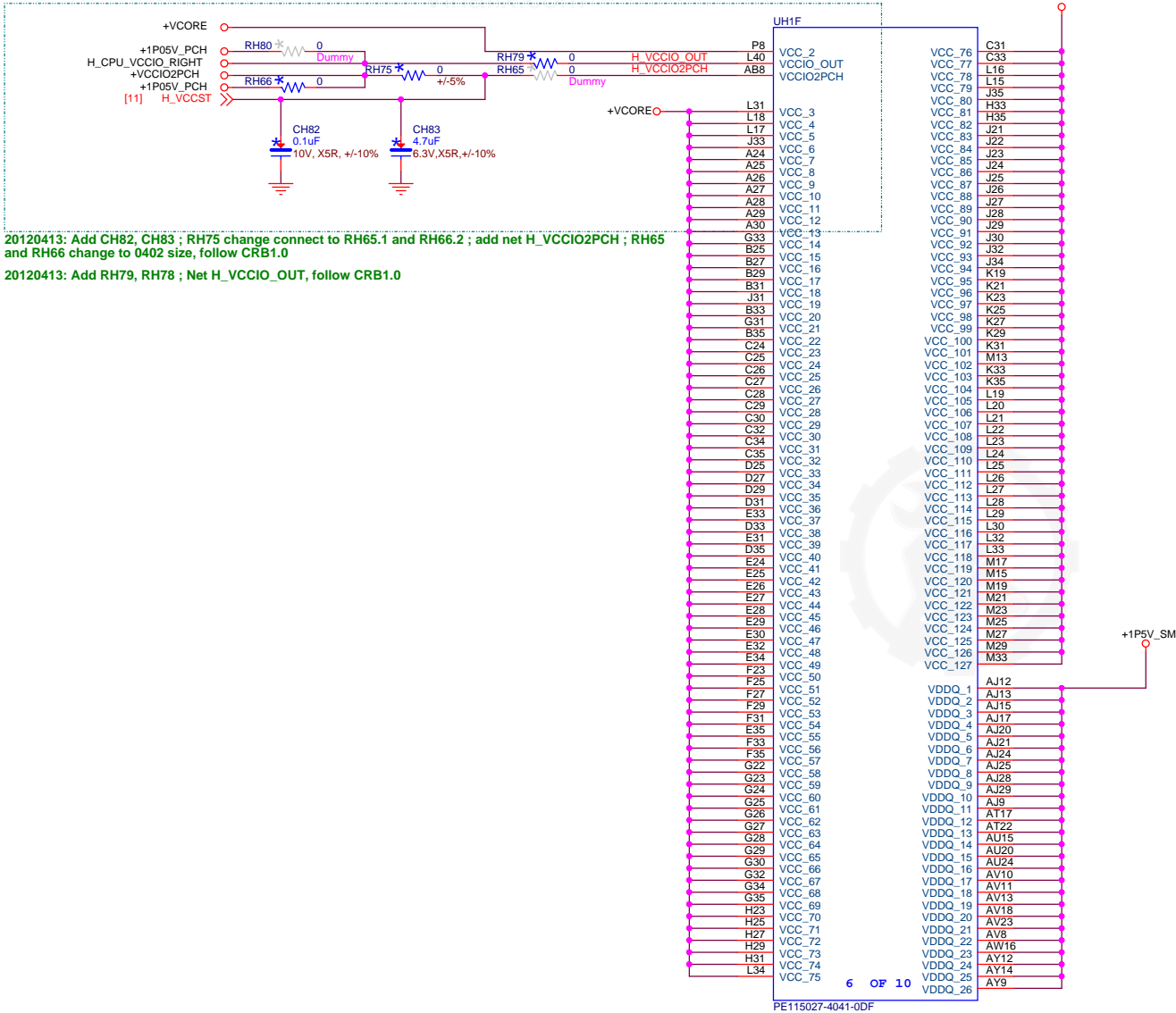


For Thunderbolt display .

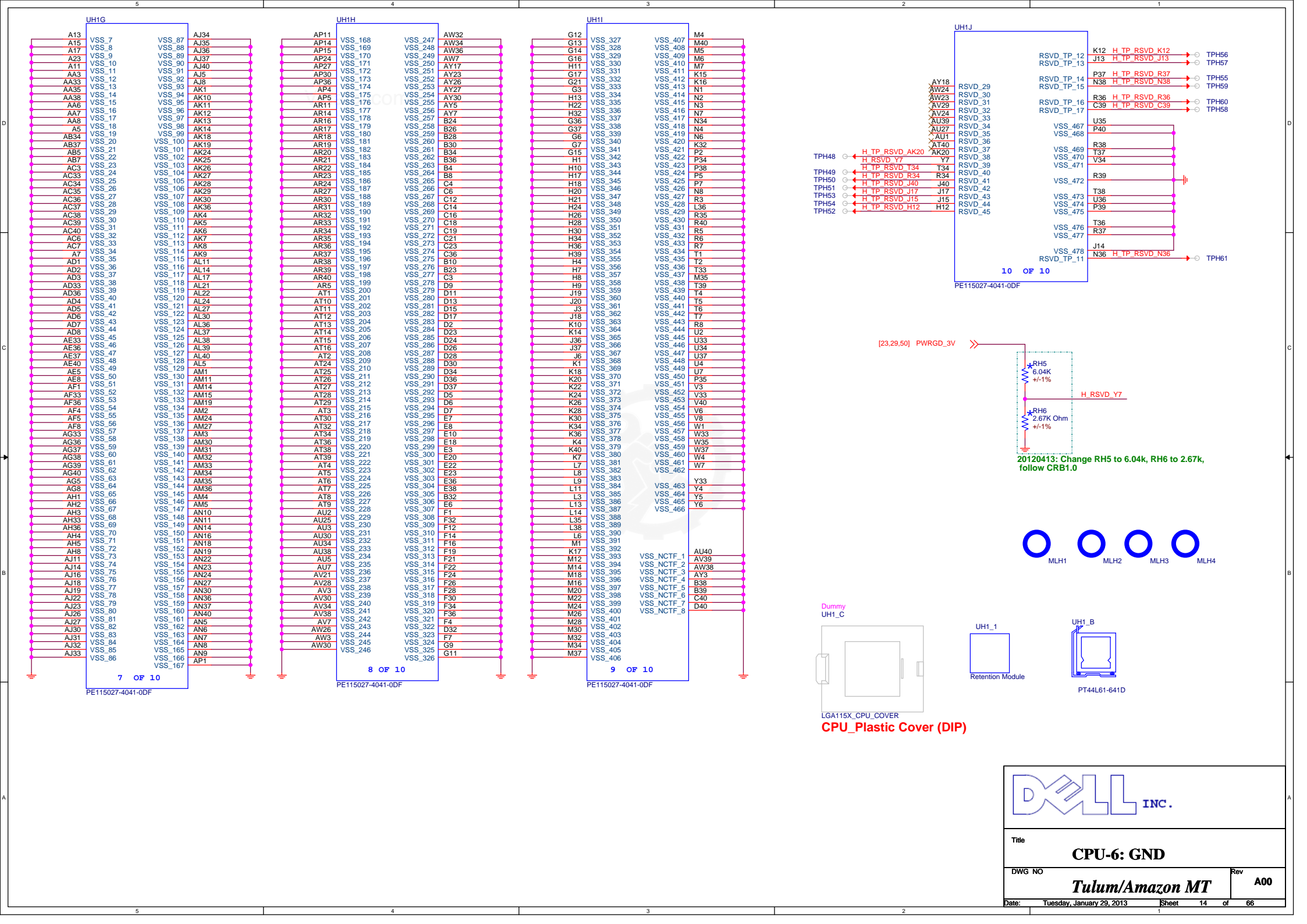
Display Port1

Display Port2

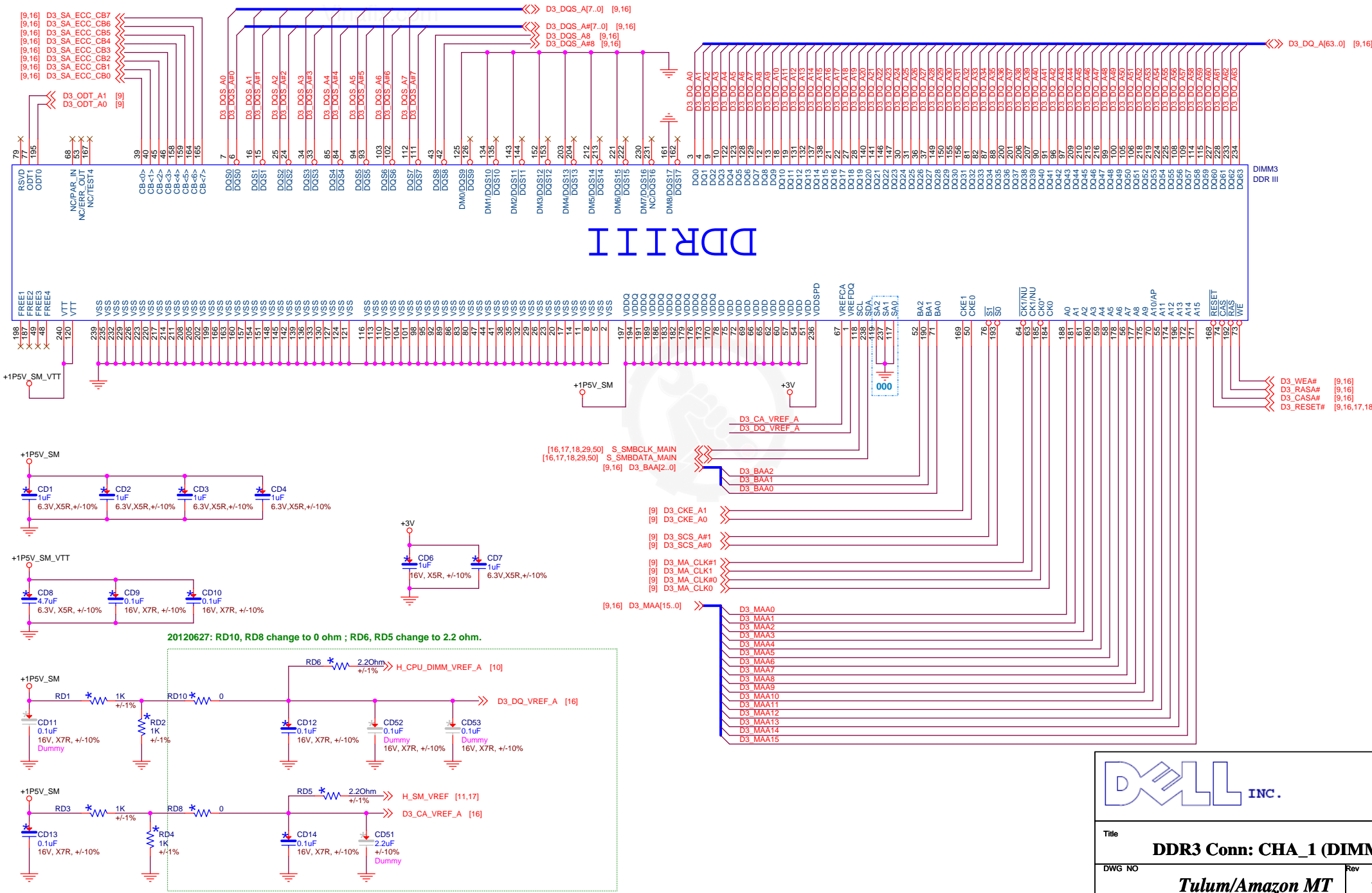
		
Title		
CPU-4: FDI/PCIe/DMI/DP		
DWG NO		Rev
	Tulum/Amazon MT	A00
Date:	Tuesday, January 29, 2013	Sheet 12 of 66



Title		
CPU-5: Vcore		
DWG NO	Tulum/Amazon MT	Rev A00
Date:	Tuesday, January 29, 2013	Sheet 13 of 66





**DDR3 Conn: CHA\_1 (DIMM3)**

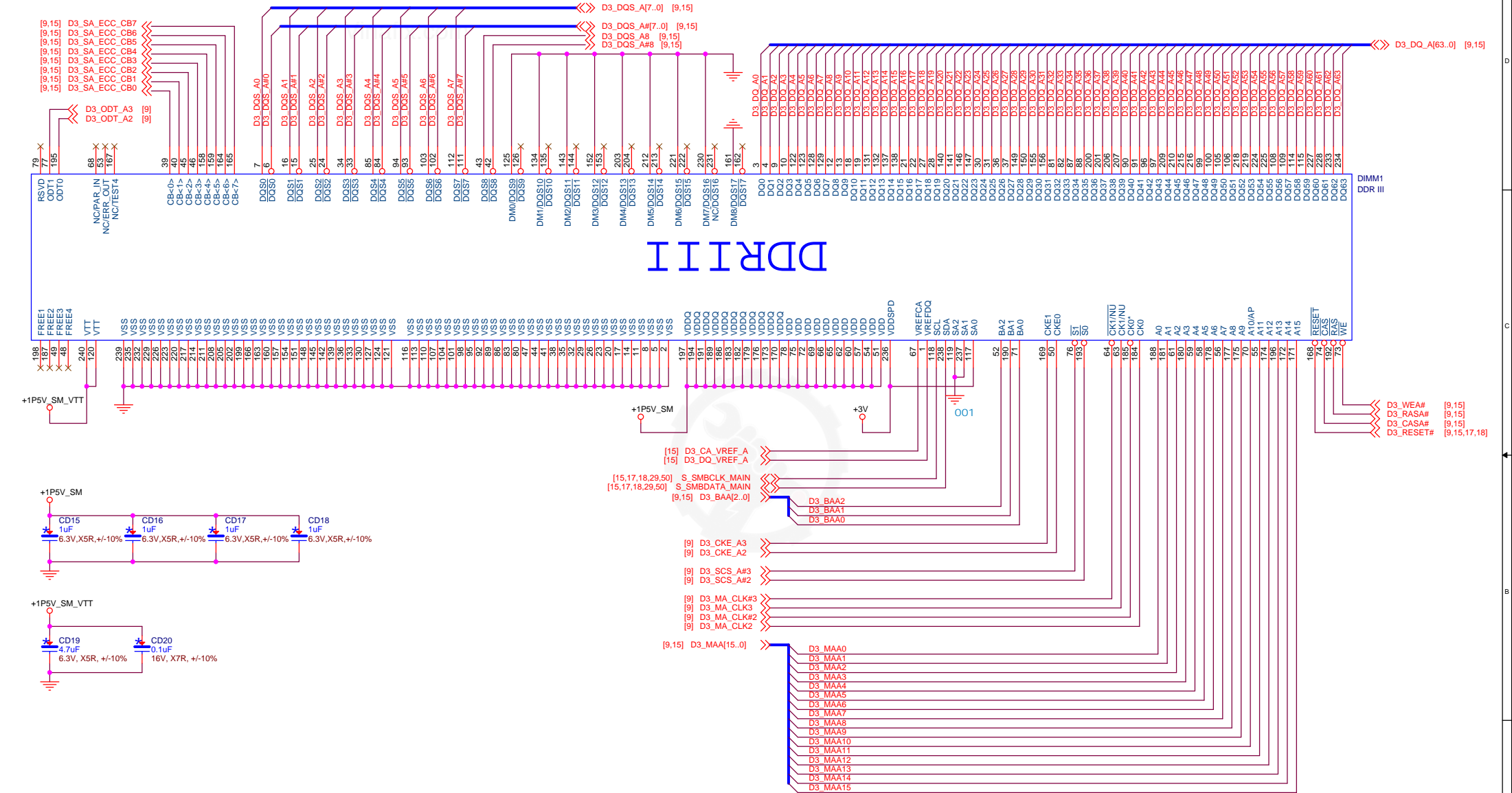
DWG NO	Rev
1	100

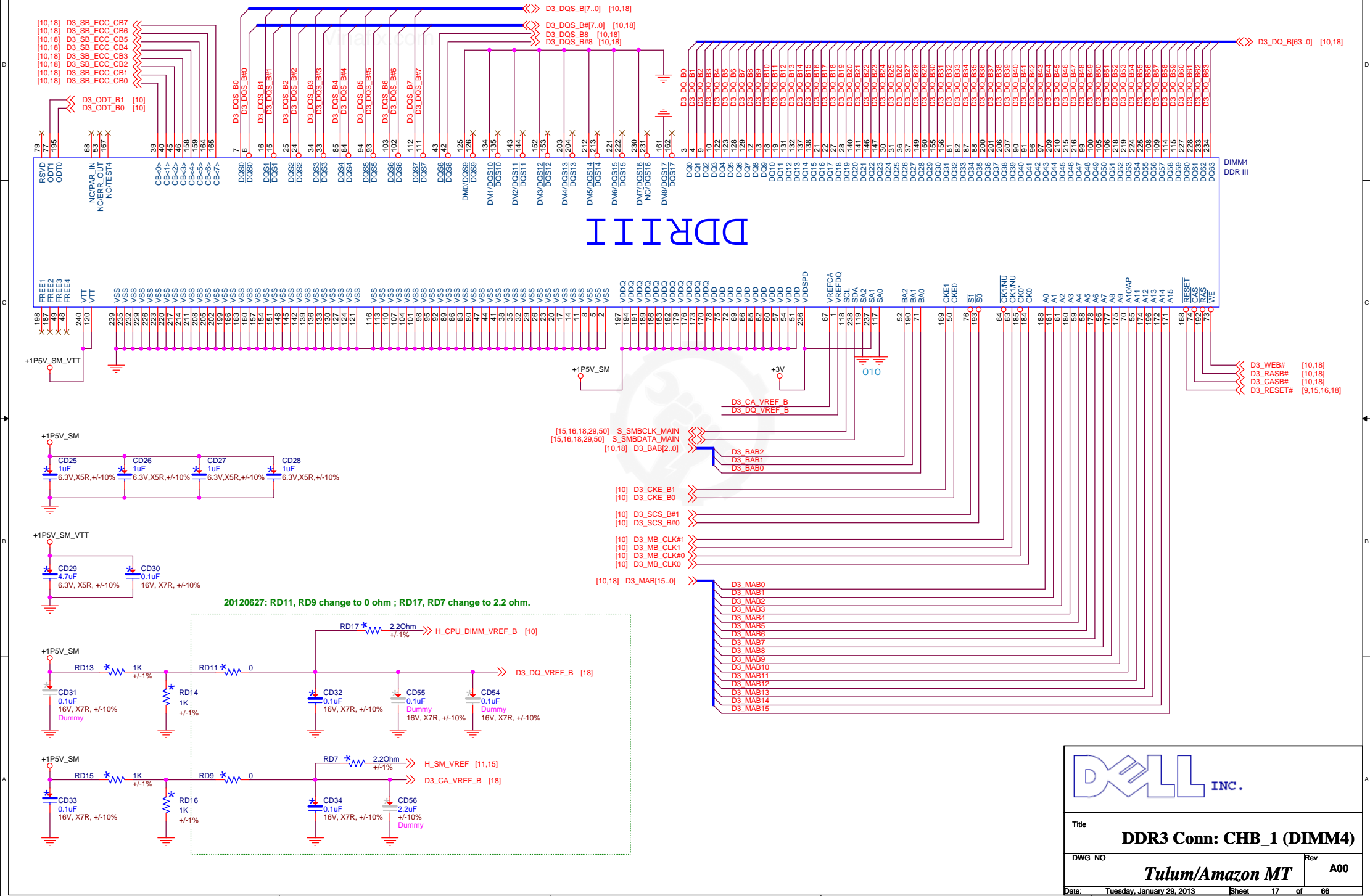
## ***Tulum/Amazon MT***

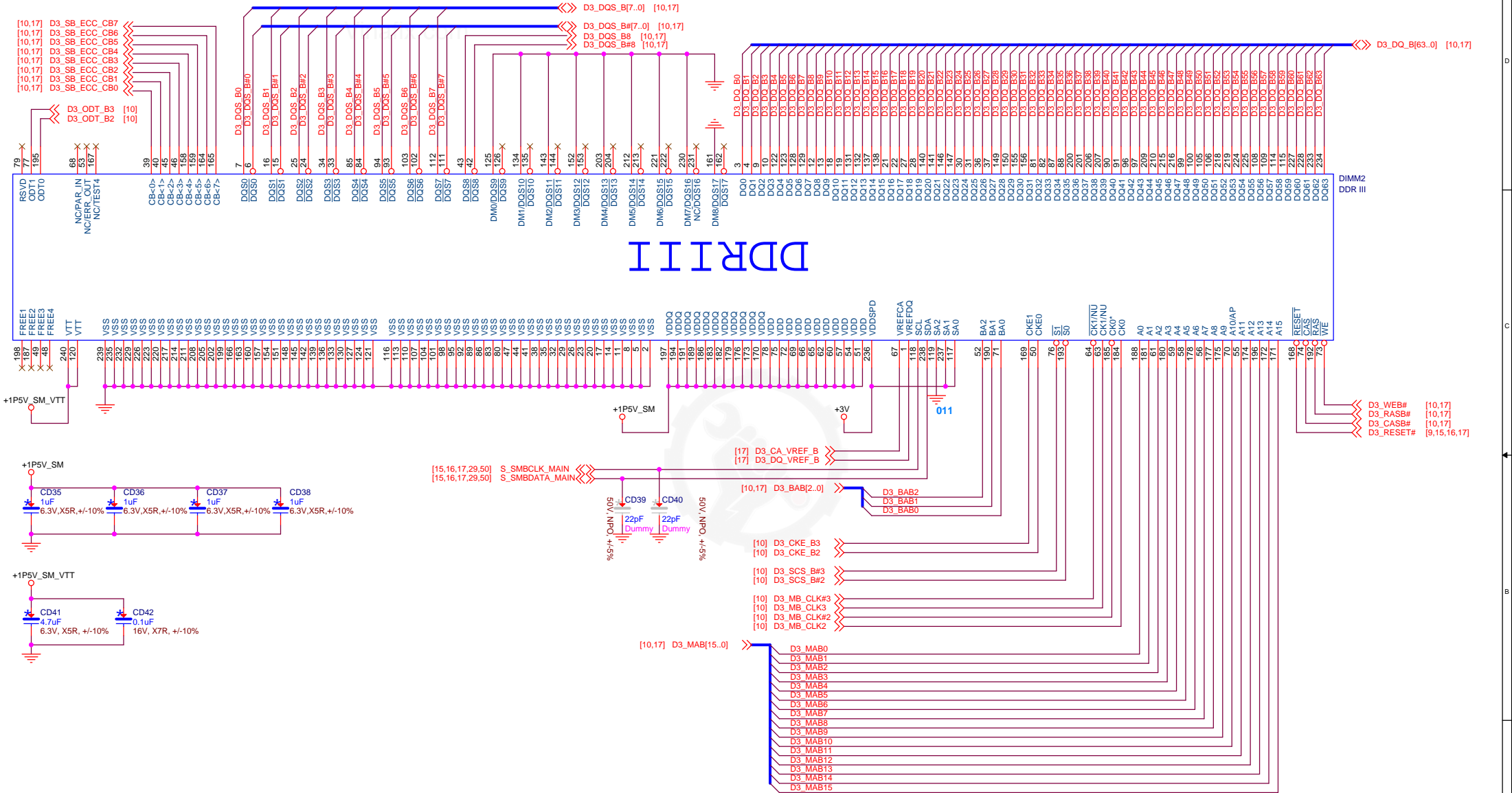
A00

66









Title			
<b>DDR3 Conn: CHB_2 (DIMM2)</b>			
DWG NO	<i>Tulum/Amazon MT</i>		Rev <b>A00</b>
Date: Tuesday, January 29, 2013	Sheet	18	of 66

5

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Vinafix.com



<LBL>  
2D-Label  
Lable



Title		Label	
DWG NO		Tulum/Amazon MT	Rev A00
Date:	Tuesday, January 29, 2013	Sheet	19 of 66

5

4

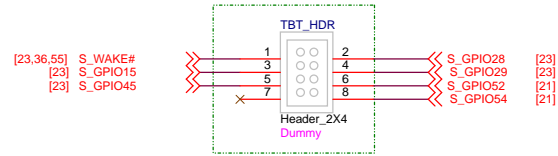
3

2

1

Vina

20120626: Add TBT\_HDR  
20120703: TBT\_HDR compoment  
REMARK cahnge to Remark



Title

**TBT\_HDR**

DWG NO

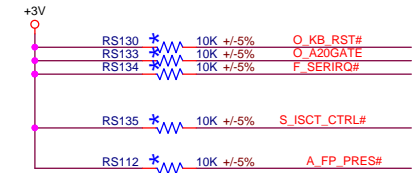
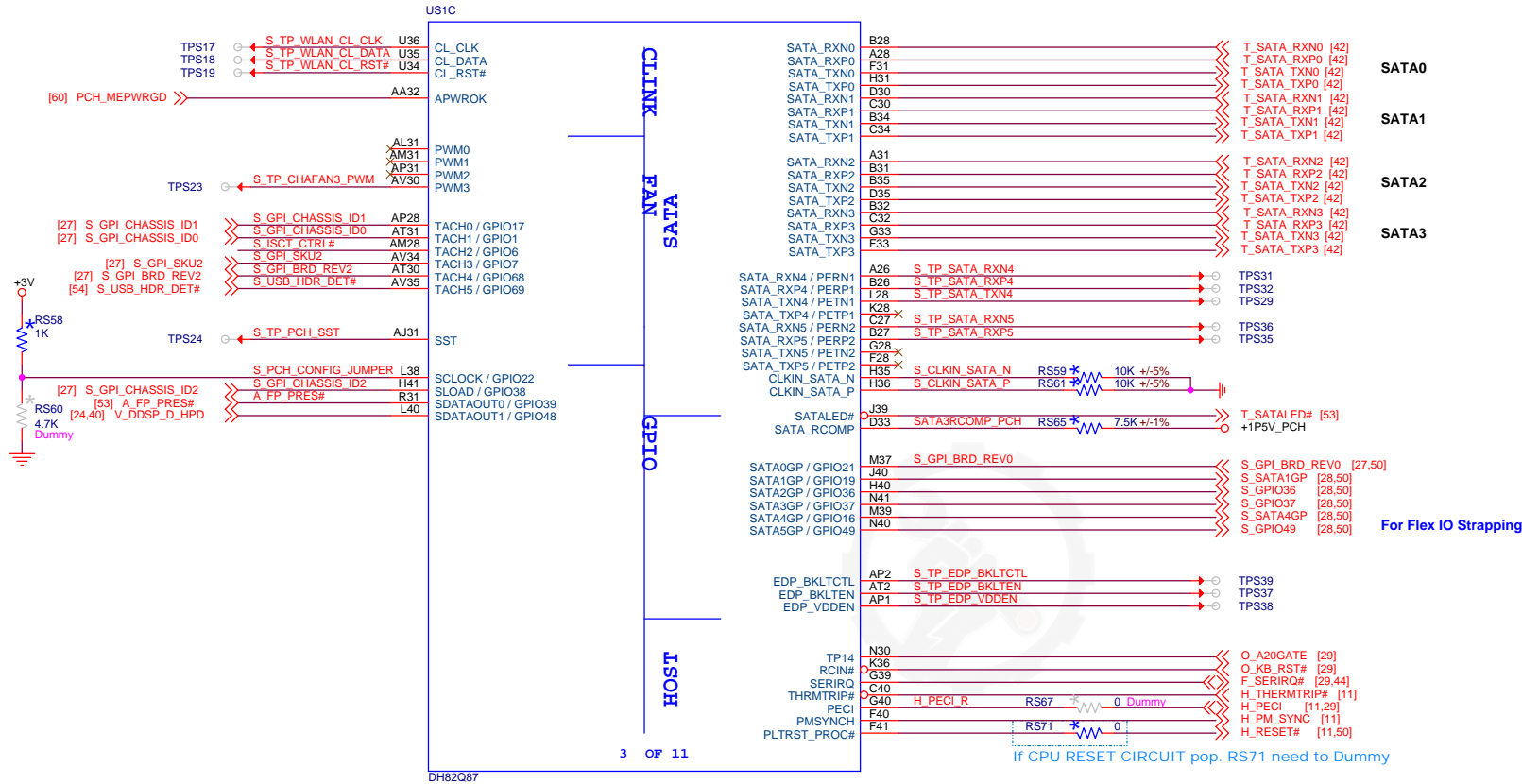
**Tulum/Amazon MT**

Rev  
**A00**

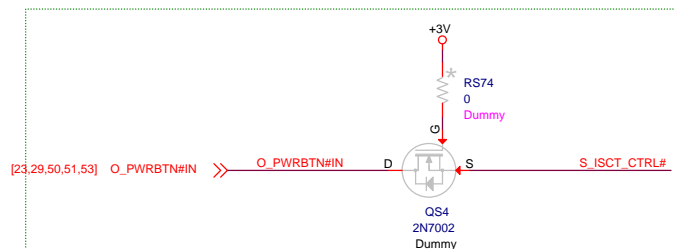
Date: Tuesday, January 29, 2013

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20120625: Add QS4 and S\_ISCT\_CTRL#



INC.

Title

**PCH-2: SATA/HOST/GPIO**

DWG NO

**Tulum/Amazon MT**

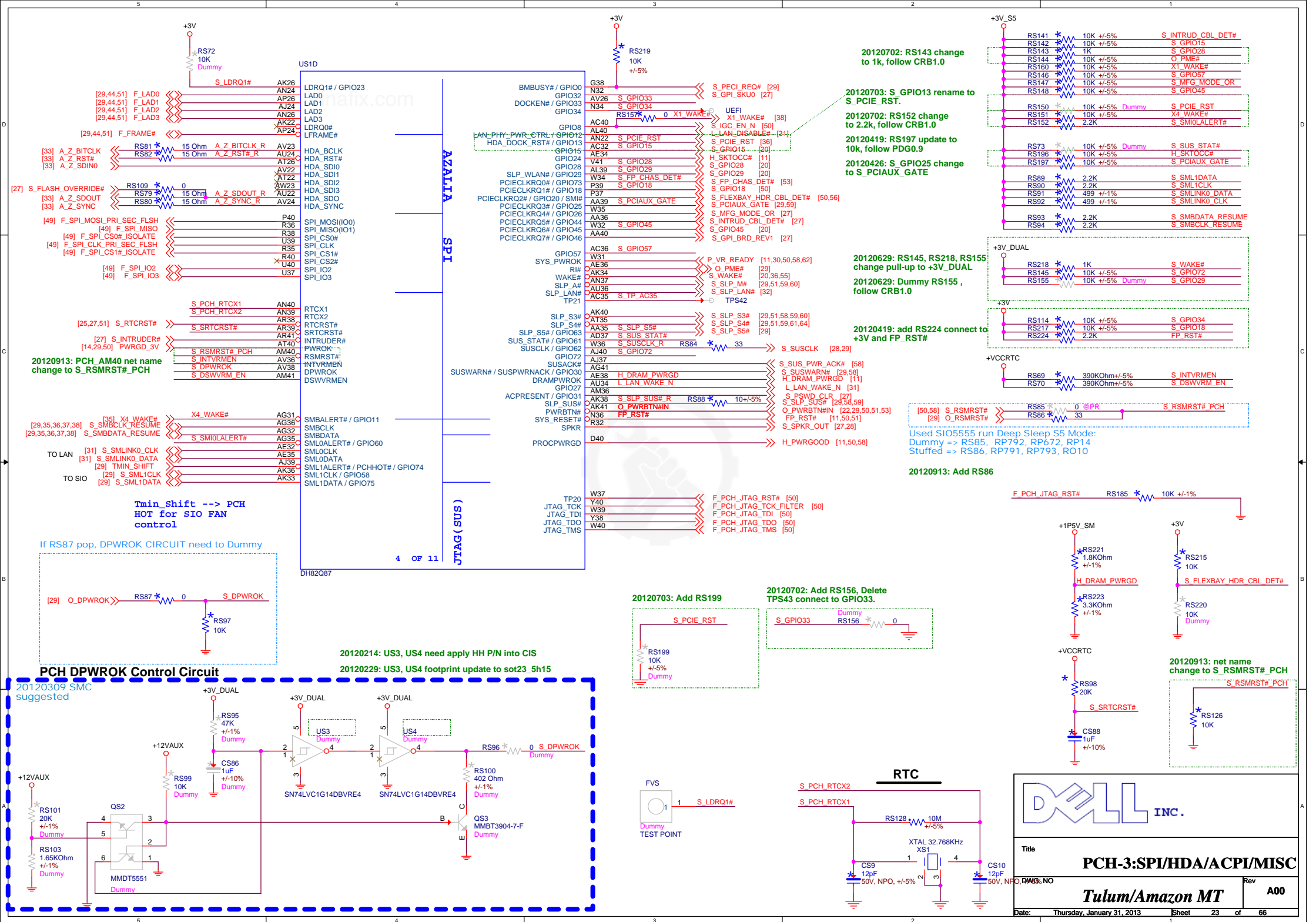
Rev

**A00**

Date: Thursday, January 31, 2013

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## US1G



## US1E

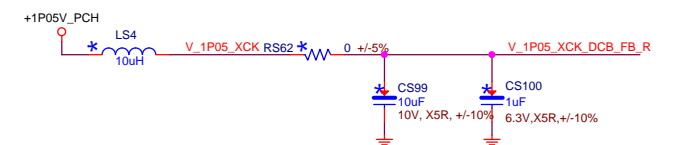
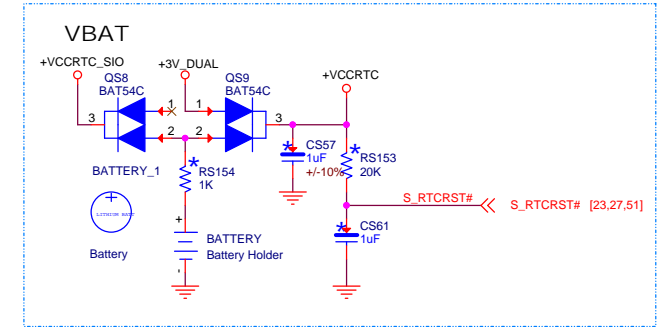
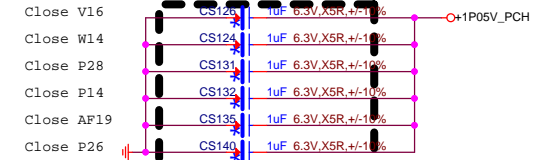
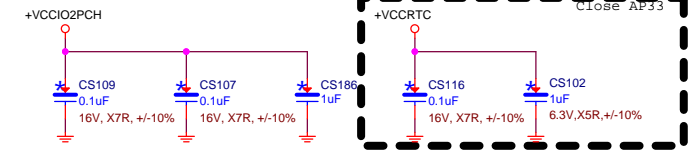
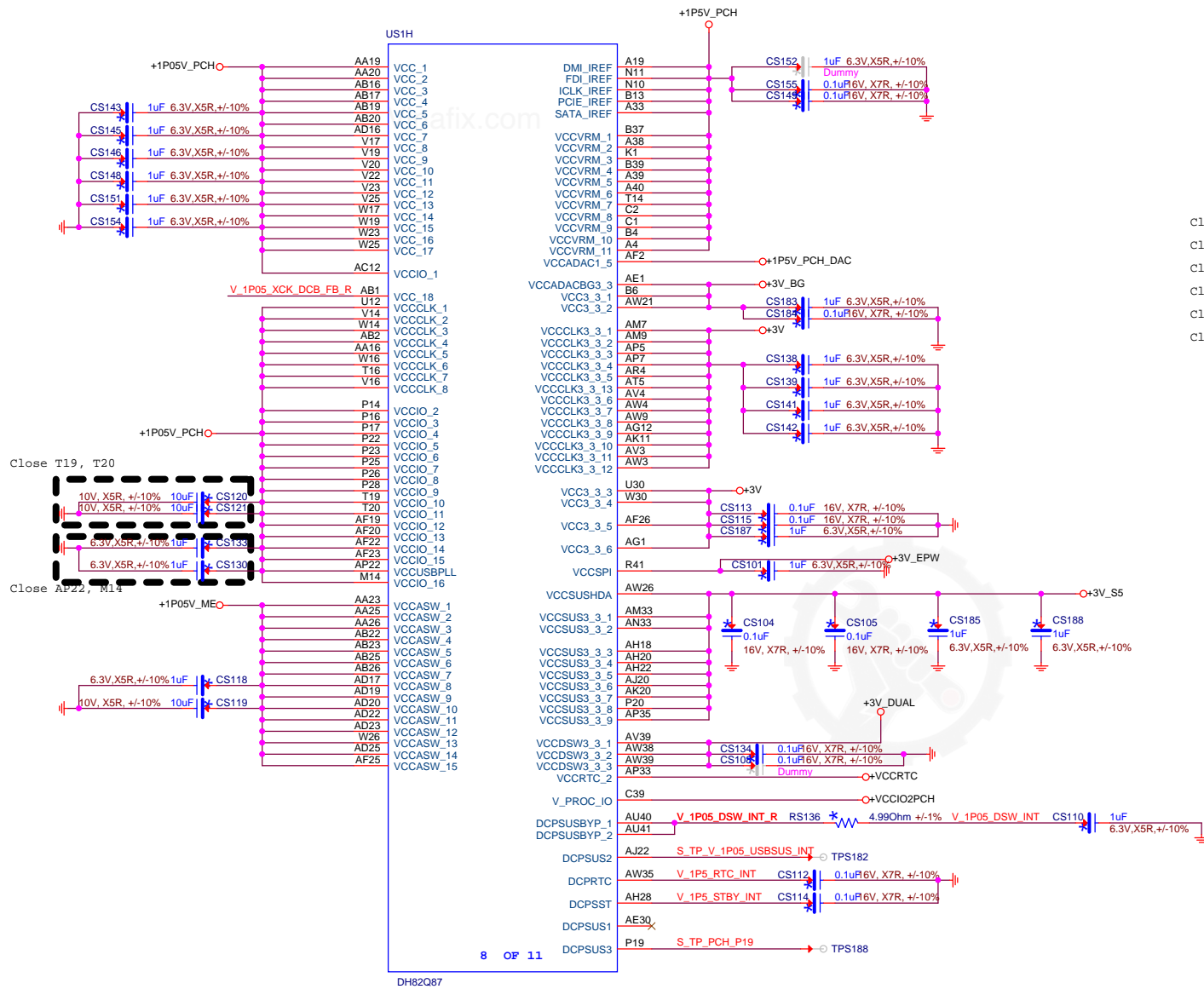


### PCH-4: VGA/USB3/CLK/FDI

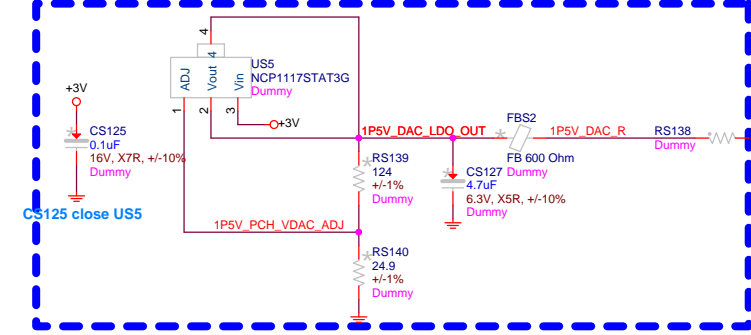
***Tulum/Amazon MT***

Rev	<b>A00</b>
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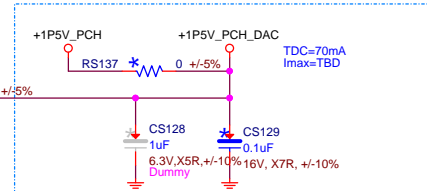
Sheet 24 of 66

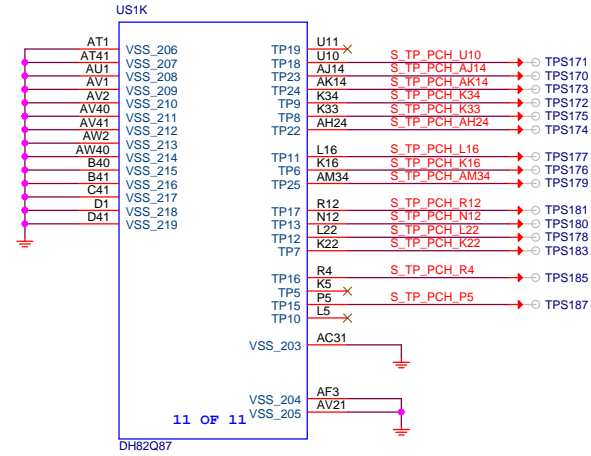
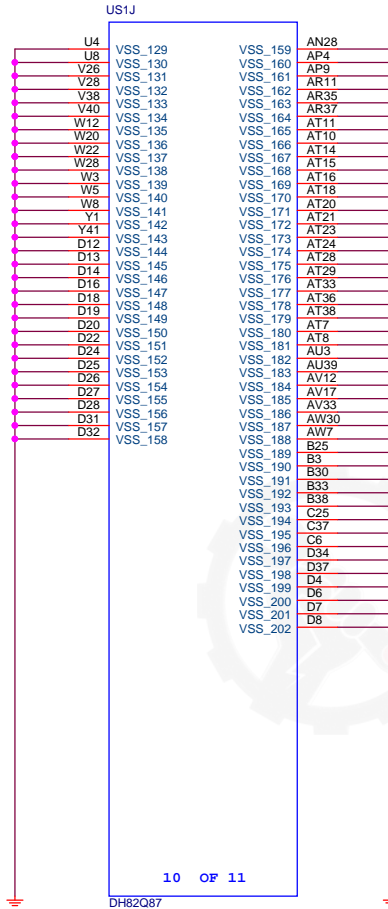
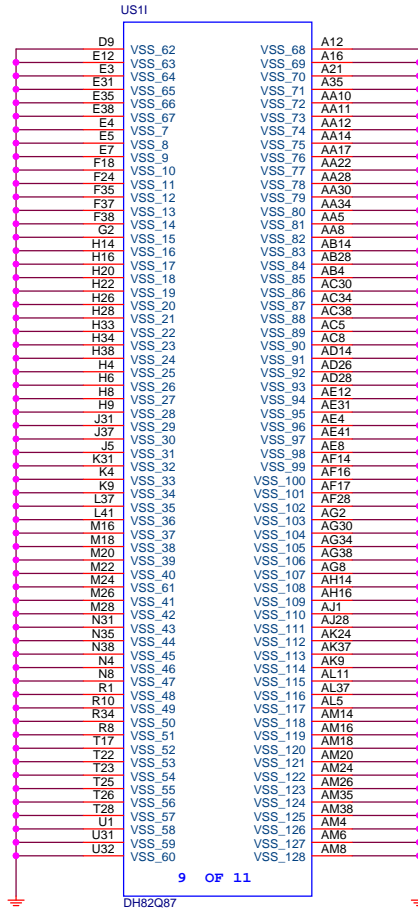


**+1P5V\_PCH\_DAC Circuit**



If RS137 pop, RS138 and +1P5V\_PCH\_DAC CIRCUIT need to Dummy





Title

**PCH-6: GND**

DWG NO

**Tulum/Amazon MT**

Rev

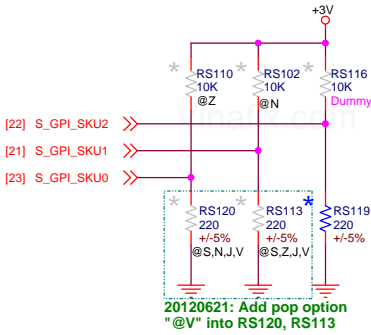
**A00**

Date: Thursday, January 31, 2013

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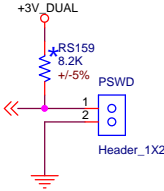
SKU ID

SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	NO TPM/NO TCM
1	1	Reserved

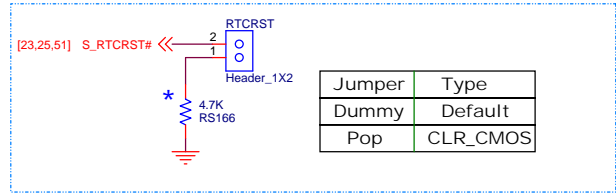


Clear Password

1-2: NORMAL  
EMPTY: CLEAR PASSWORD

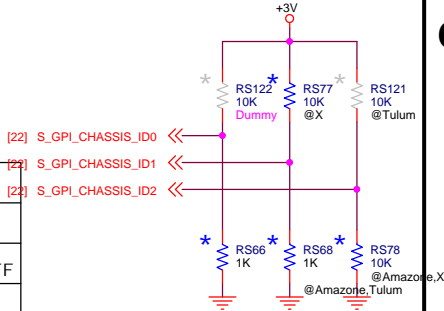


CLR\_CMOS

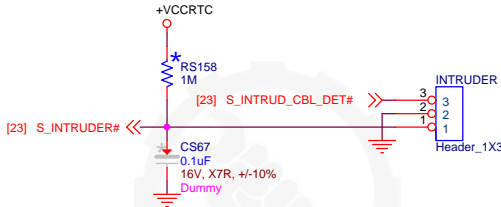


Chassis ID

ID2	ID1	ID0	Type
1	0	1	SFF
1	1	0	Tulum SFF
1	1	1	X-SFF
0	0	0	MT
1	0	0	Tulum MT
0	1	0	X-MT
0	1	1	USFF

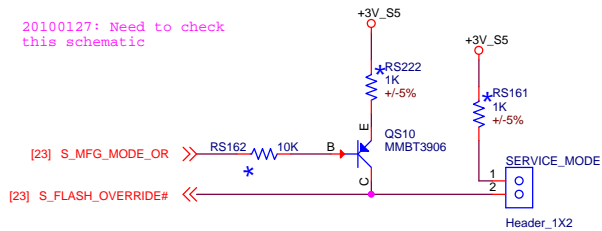


Chassis Intruder



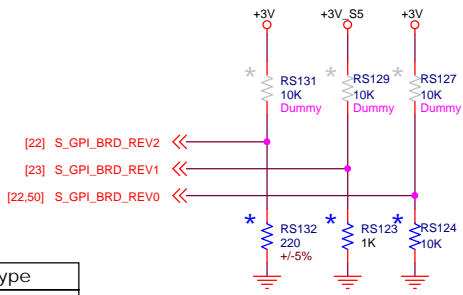
ME Disable (Flash override)

20100127: Need to check this schematic

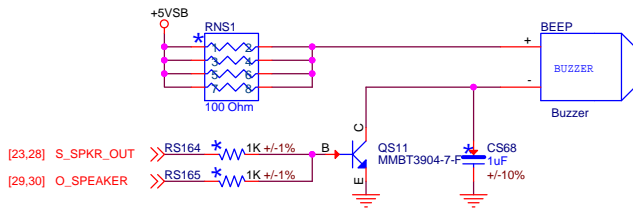


BOARD ID

Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



BEEP



Title

DWG NO

Date: Tuesday, January 29, 2013

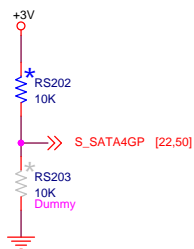
PCH-8: MISC CONN/BEEP/ID

Tulum/Amazon MT

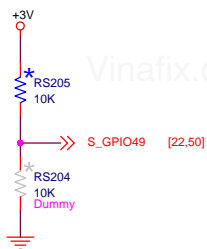
Rev A00

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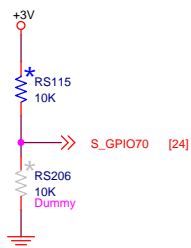
GPIO16 (H--&gt;SATA4 ; L--&gt;PCle1)



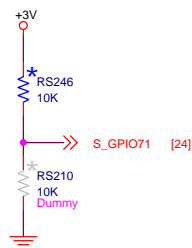
GPIO49 (H--&gt;SATA5 ; L--&gt;PCle2)



GPIO70 (H--&gt;PCle1 ; L--&gt;USB3 3)

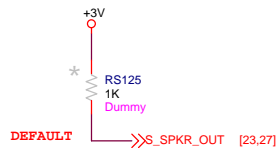


GPIO71 (H--&gt;PCle2 ; L--&gt;USB3 4)



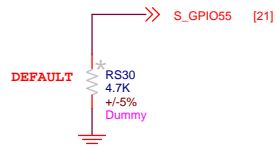
No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable



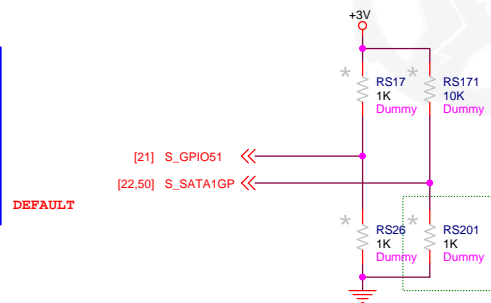
Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable



Boot BIOS Destination Selection

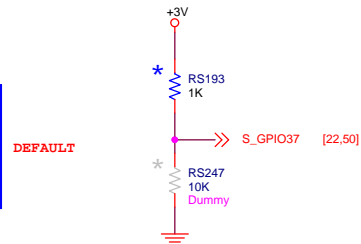
GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI



20120524: RS201 change to 1k, follow PDG1.0

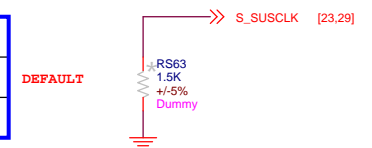
TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality



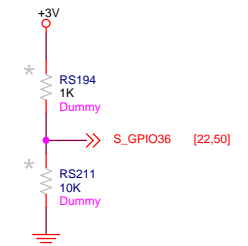
On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.



DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW



Title

PCH-9: STRAP OPTION

DWG NO

Tulum/Amazon MT

Rev

A00

Date: Tuesday, January 29, 2013

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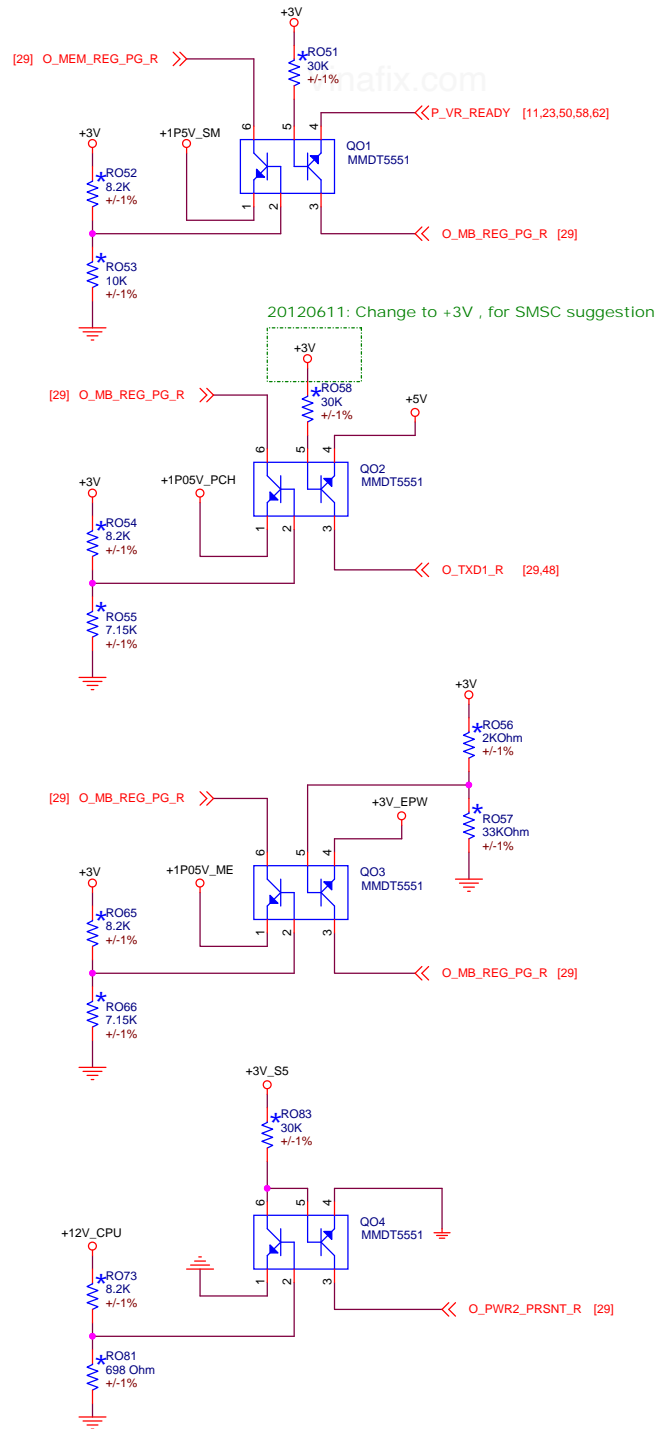


20120502: UO1 change to  
SCH5555-NS B, version B.

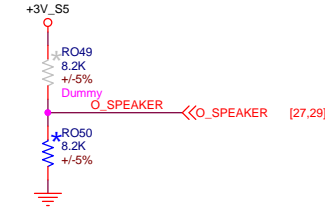




## 5555 PRE-POST DIAG Monitor



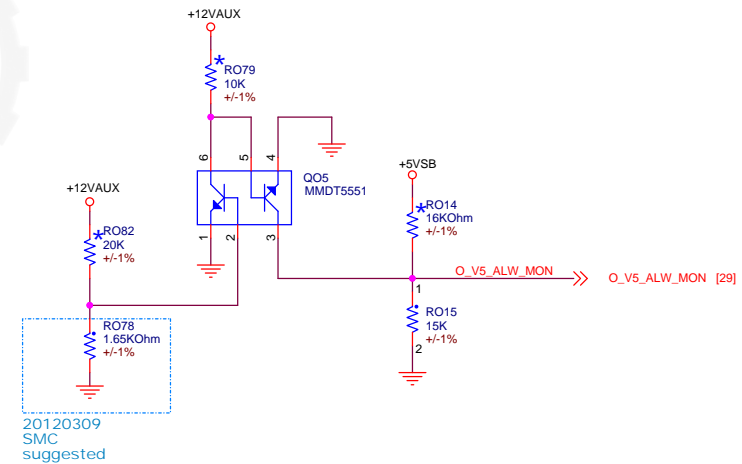
## SIO STRAPING



SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

## SIO5555 V5\_ALW Monitor

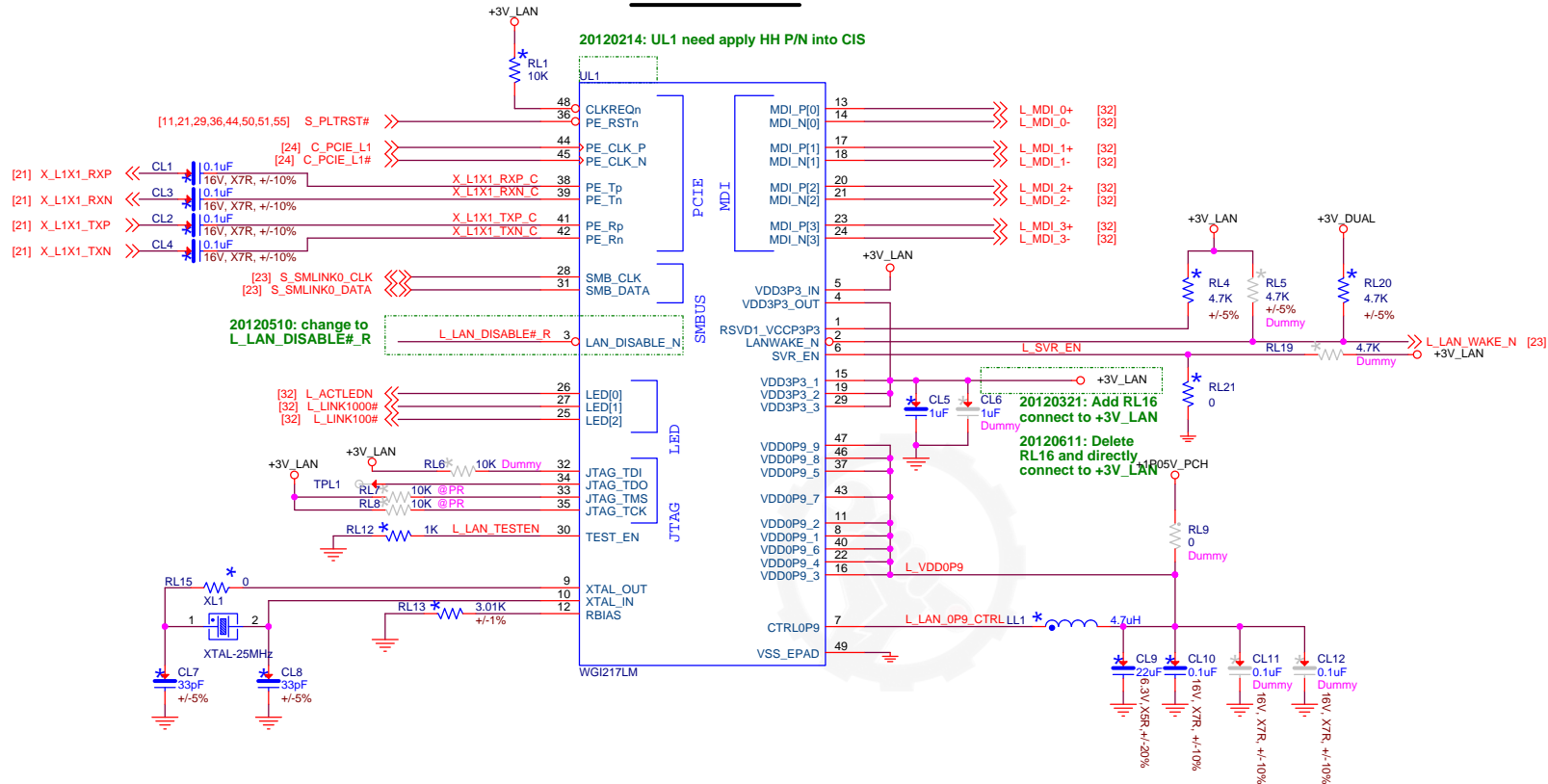


Title		
SIO-SCH5555-2		
DWG NO	Tulum/Amazon MT	Rev A00
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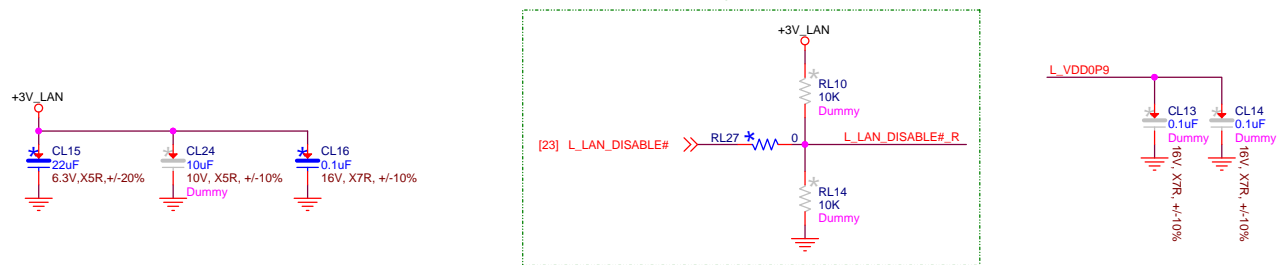
Vinafix.cc **Clarkville need applied CIS.**

## Intel Clarkville

20120214: UL1 need apply HH P/N into CIS



**20120510: Add RL27 ; Dummy RL10 , follow CRB1.0**



Title
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**LAN: Intel Clarkville**

DWG NO
--------

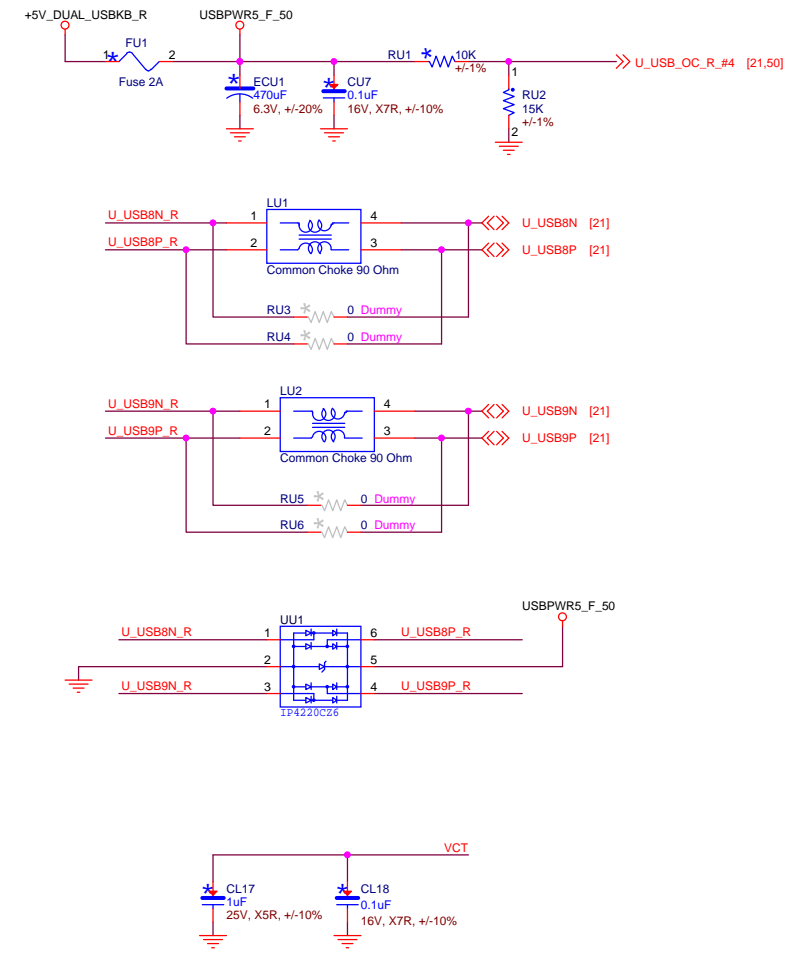
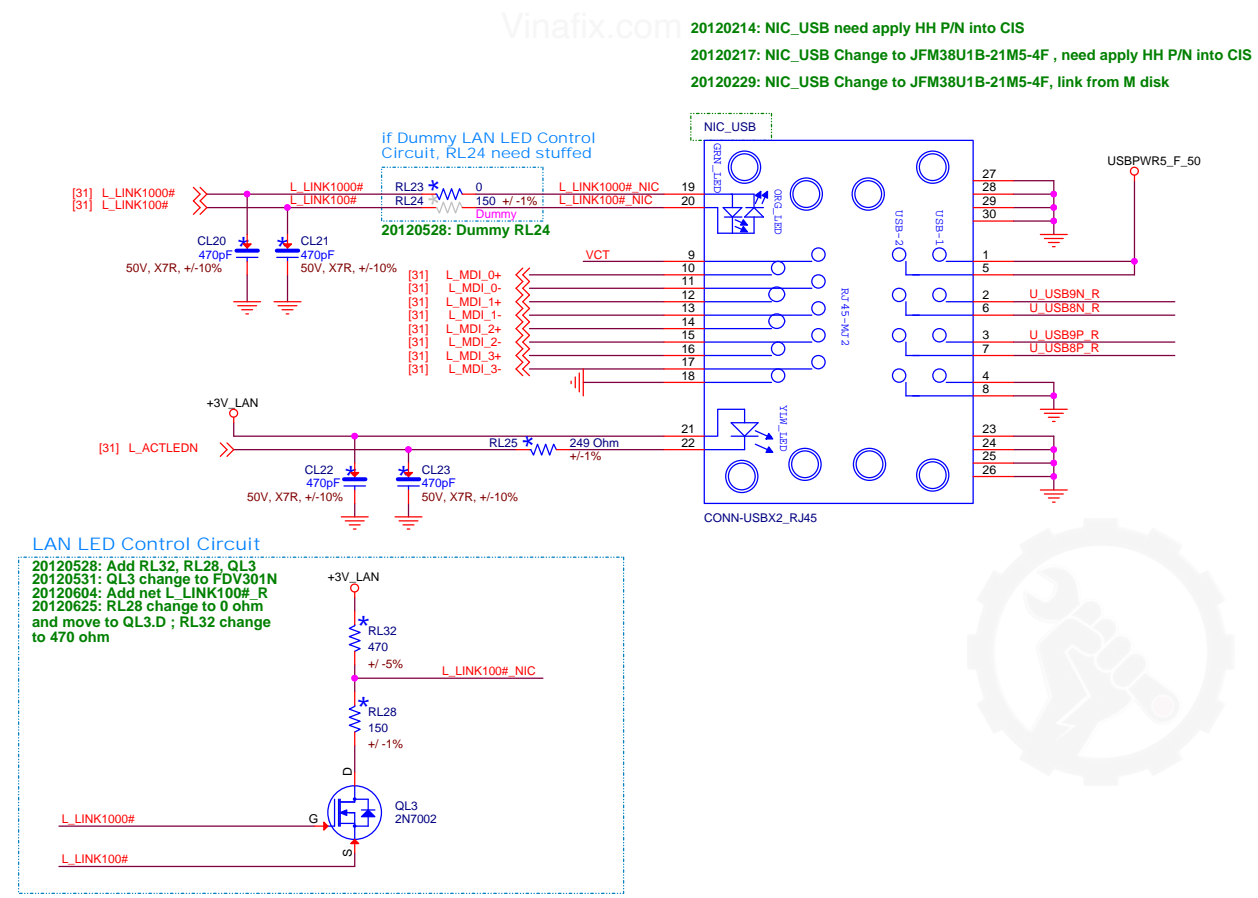
***Tulum/Amazon MT***

Rev	<b>A00</b>
-----	------------

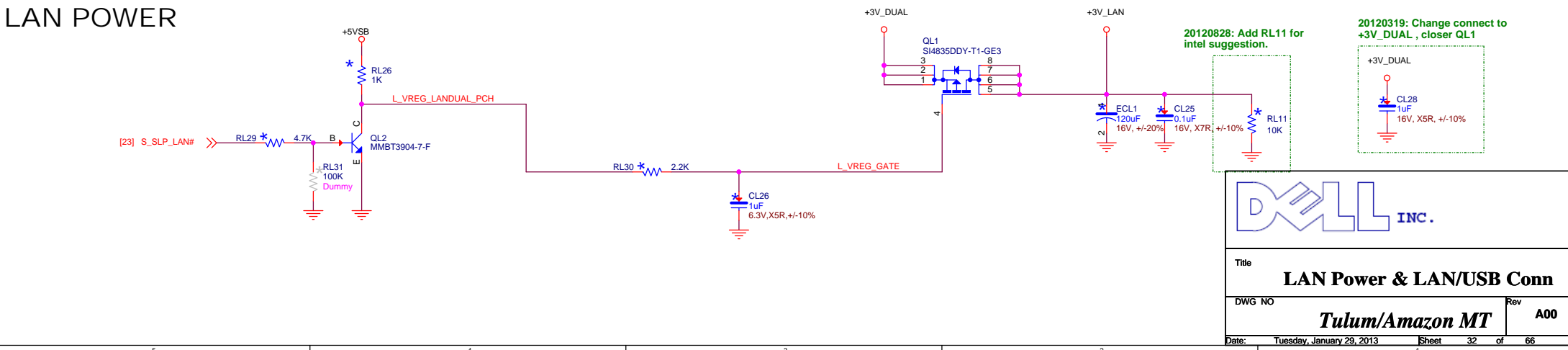
Date: Tuesday, January 29, 2013

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# LAN CONNECTOR



# LAN POWER

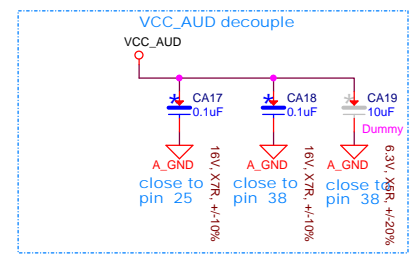
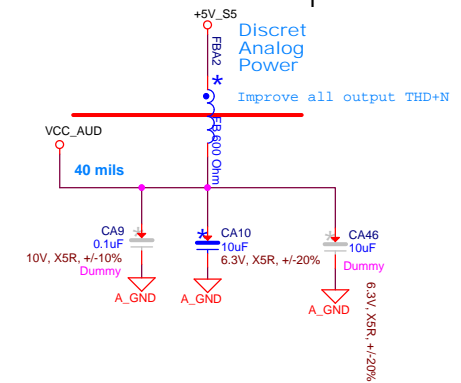
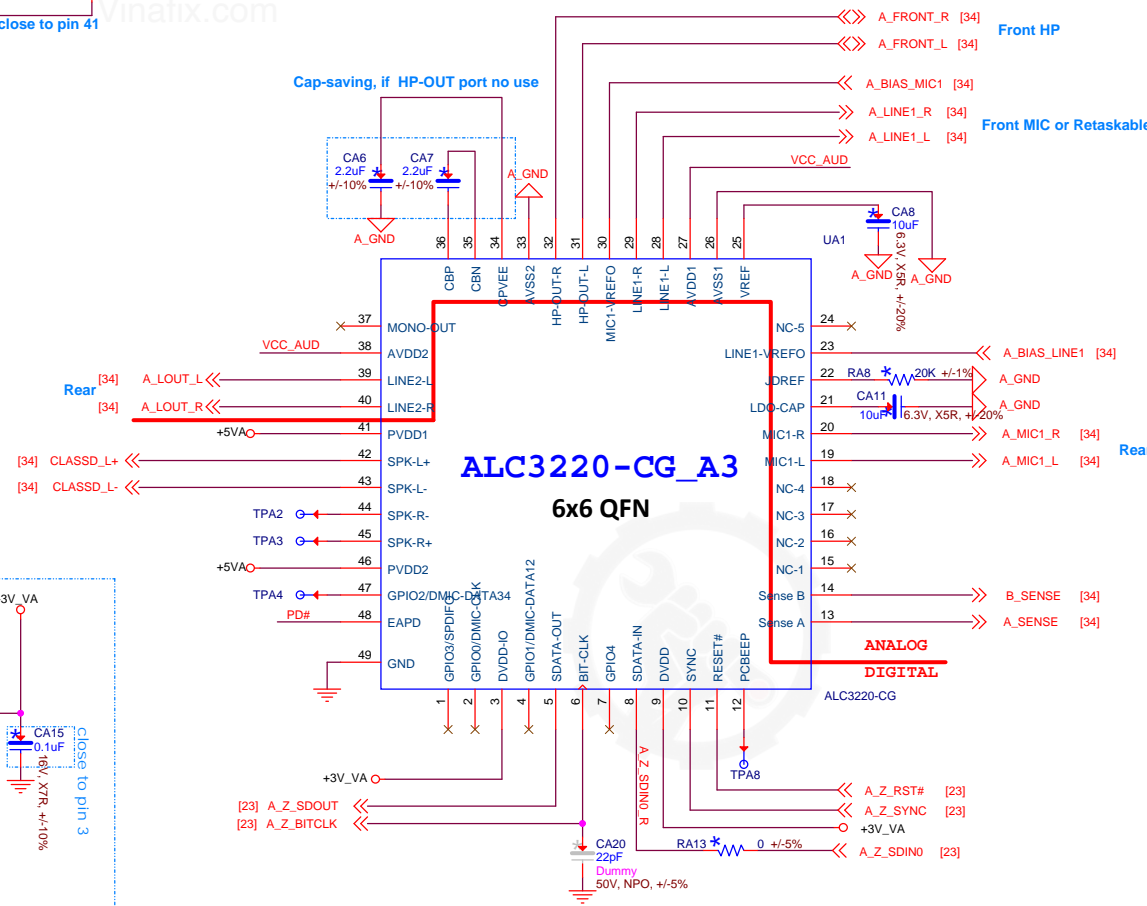
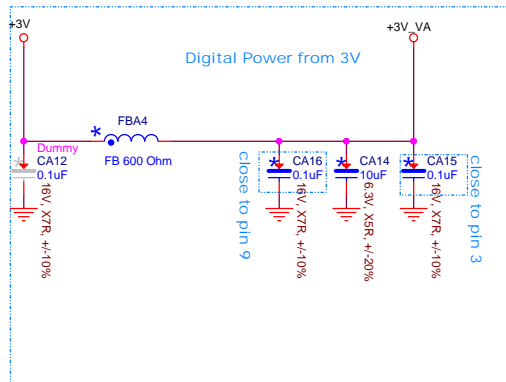
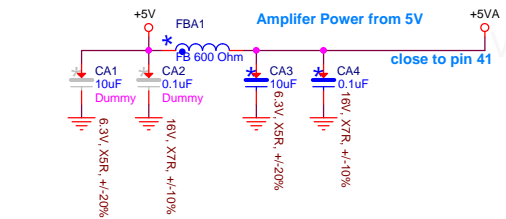


**DELL INC.**

Title: LAN Power & LAN/USB Conn

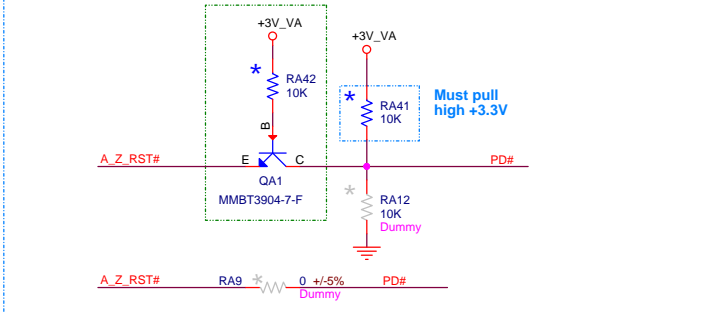
DWG NO: Tulum/Amazon MT Rev: A00

Date: Tuesday, January 29, 2013 Sheet: 32 of 66

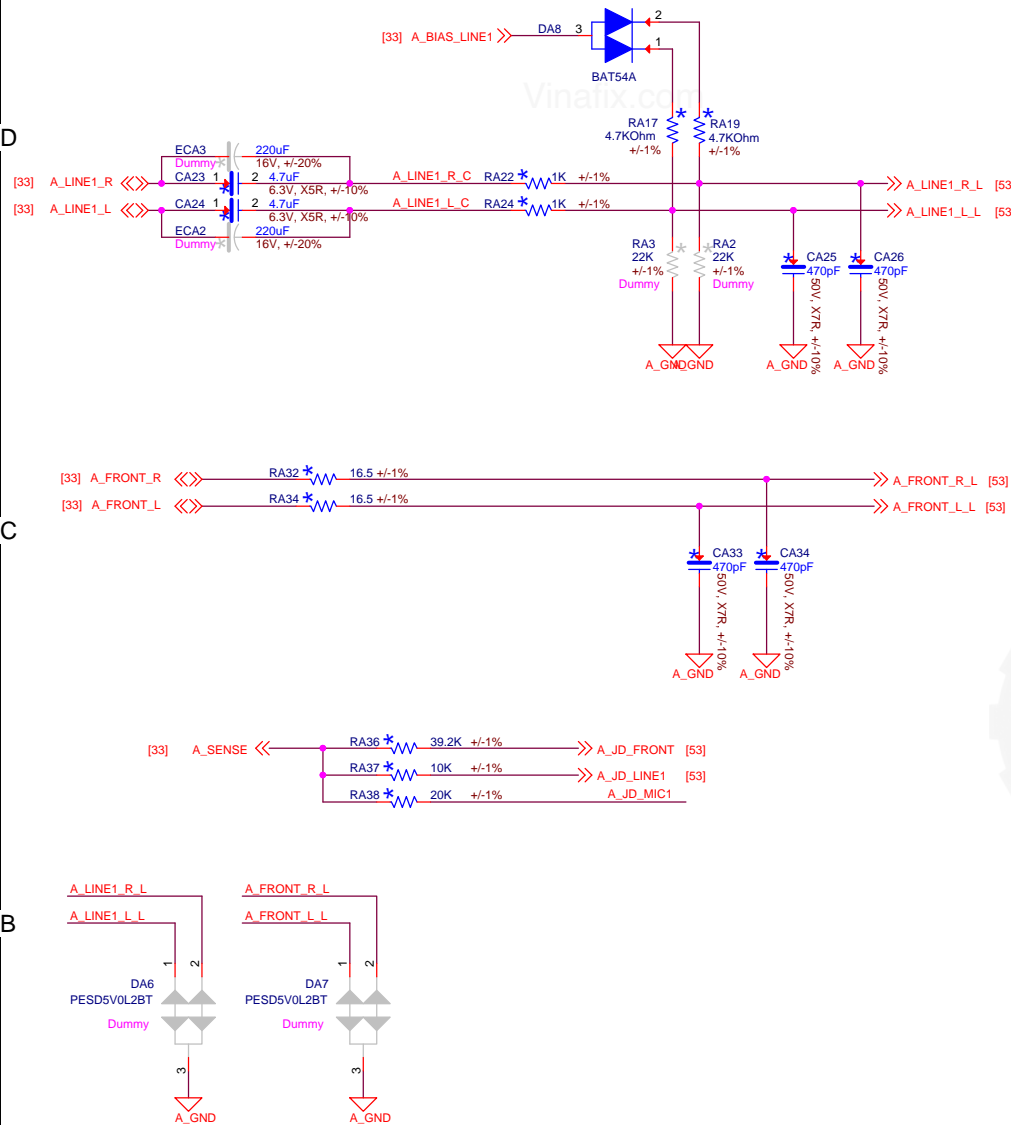


20120424 for solve AZ\_RST and EAPD issue

20120517: QA1 change to MMBT3904-7-F ; add RA42 and connect to +3V\_VA

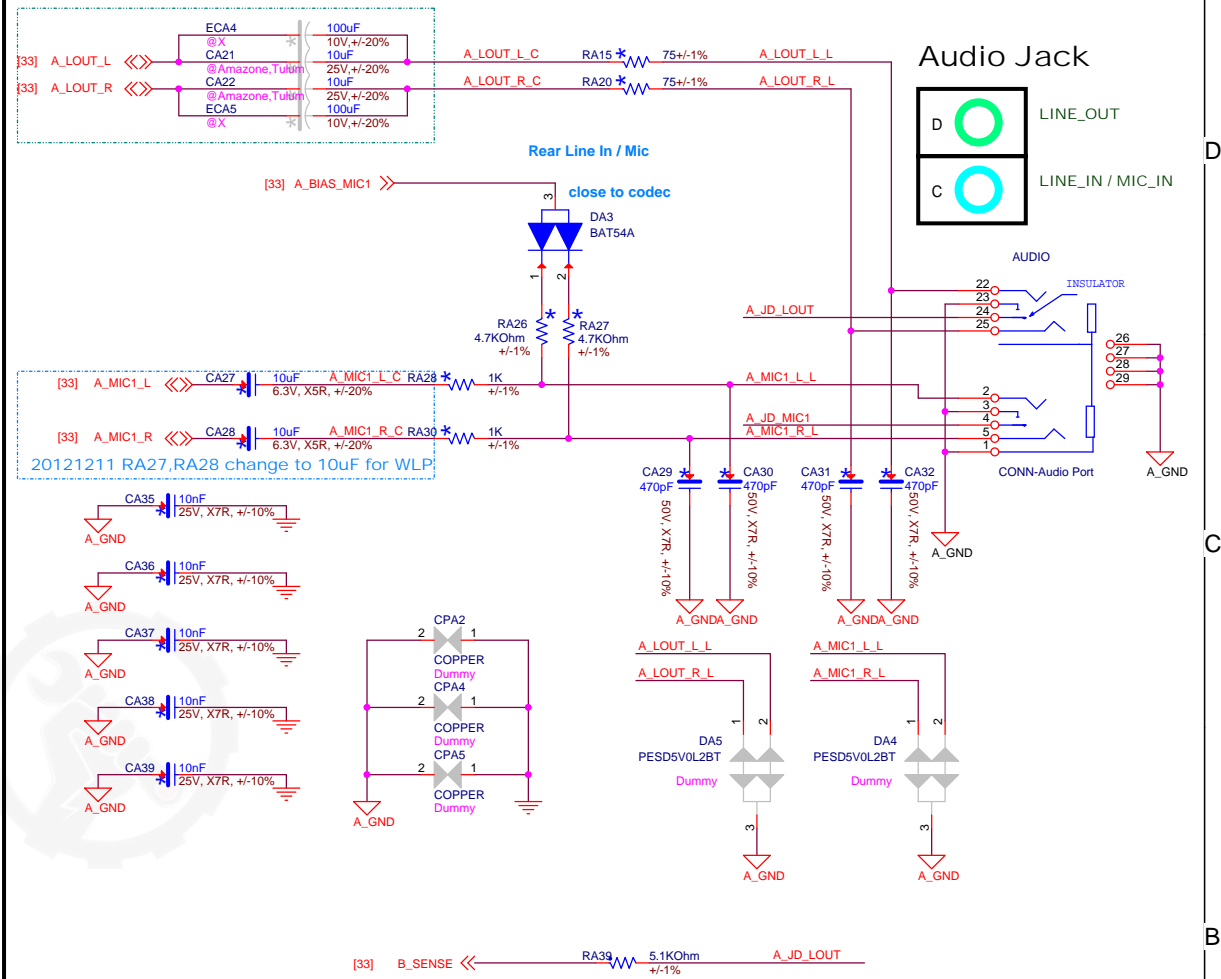


# Front Audio



20120626: Add ECA4 co-layer with CA21 : ECA5 co-layer with CA22  
20120829: ECA4, ECA5 change to 100uF and CA21, CA22 add remark option

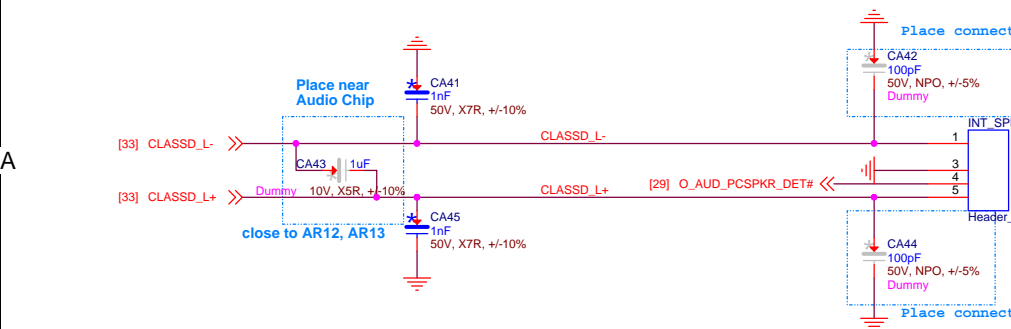
# Rear Audio Jack



# CHASSIS SPEAKER

Header 1x5 cut2

Pin.1--> Left-  
Pin.2--> NC key  
Pin.3--> GND  
Pin.4--> SPK det#  
Pin.5--> Left+



Title		
Audio Conn		
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[12] X\_1X16\_TXP[15..0] >>  
[12] X\_1X16\_TXN[15..0] >>

[23,29,35,37,38] S\_SMBCLK\_RESUME >>  
[23,29,35,37,38] S\_SMBDATA\_RESUME >>

[20,23,55] S\_WAKE# <<

X\_1X16\_TXP0 CX45 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP0  
X\_1X16\_TXN0 CX46 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN0

X\_1X16\_TXP1 CX66 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP1  
X\_1X16\_TXN1 CX73 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN1

X\_1X16\_TXP2 CX44 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP2  
X\_1X16\_TXN2 CX53 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN2

X\_1X16\_TXP3 CX63 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP3  
X\_1X16\_TXN3 CX72 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN3

X\_1X16\_TXP4 CX78 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP4  
X\_1X16\_TXN4 CX49 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN4

X\_1X16\_TXP5 CX50 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP5  
X\_1X16\_TXN5 CX64 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN5

X\_1X16\_TXP6 CX71 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP6  
X\_1X16\_TXN6 CX79 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN6

X\_1X16\_TXP7 CX47 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP7  
X\_1X16\_TXN7 CX54 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN7

X\_1X16\_TXP8 CX52 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP8  
X\_1X16\_TXN8 CX65 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN8

X\_1X16\_TXP9 CX82 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP9  
X\_1X16\_TXN9 CX70 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN9

X\_1X16\_TXP10 CX69 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP10  
X\_1X16\_TXN10 CX76 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN10

X\_1X16\_TXP11 CX68 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP11  
X\_1X16\_TXN11 CX75 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN11

X\_1X16\_TXP12 CX74 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP12  
X\_1X16\_TXN12 CX46 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN12

X\_1X16\_TXP13 CX43 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP13  
X\_1X16\_TXN13 CX51 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN13

X\_1X16\_TXP14 CX77 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP14  
X\_1X16\_TXN14 CX48 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN14

X\_1X16\_TXP15 CX56 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DP15  
X\_1X16\_TXN15 CX55 220nF 16V X7R +/-10% X\_EXP\_A\_TX\_C\_DN15

SLOT1

KEY

Slot-PCIe-16X

Used PCH GPIO13 PCIE RESET Mode:  
Stuffed => RX11  
Dummy => RX10

RX10 0 Dummy  
RX11 0 X\_RST\_SLOT\_PEG# X\_PLTRST\_PCIE\_SLOT# [29,35,38]

C\_PCIE16\_1 [24]  
C\_PCIE16#\_1 [24]

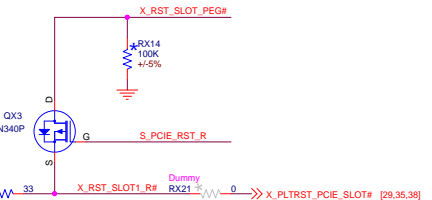
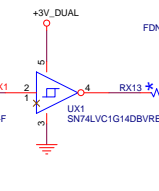
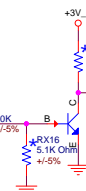
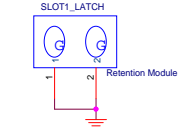
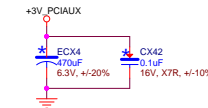
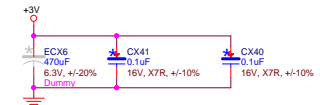
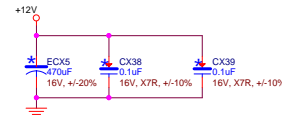
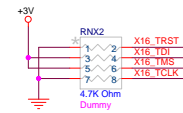
## PCIE RESET LOGIC CIRCUIT

Used PCH GPIO13 PCIE RESET Mode:  
Stuffed => RX12, RX20, RS225

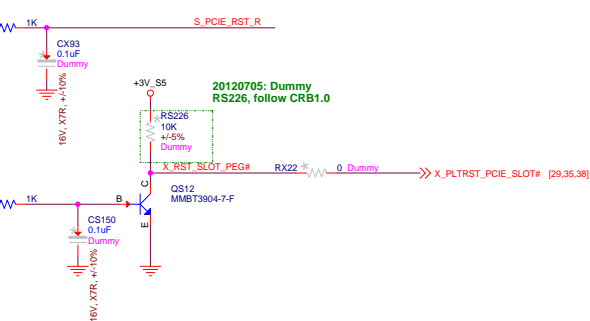
[11,21,29,31,44,50,51,55] S\_PLTRST# >>

[23] S\_PCIE\_RST >>

>> X\_1X16\_RXP[15..0] [12]  
>> X\_1X16\_RXN[15..0] [12]

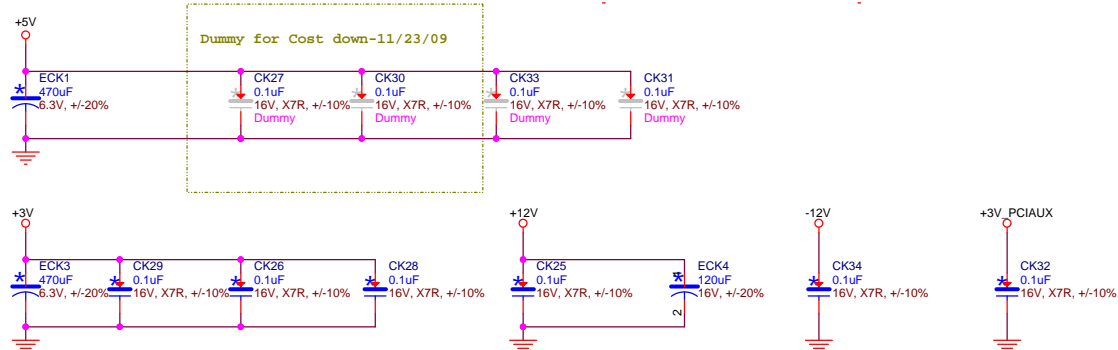
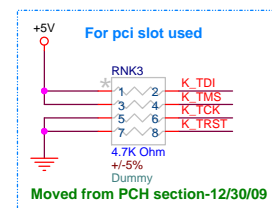
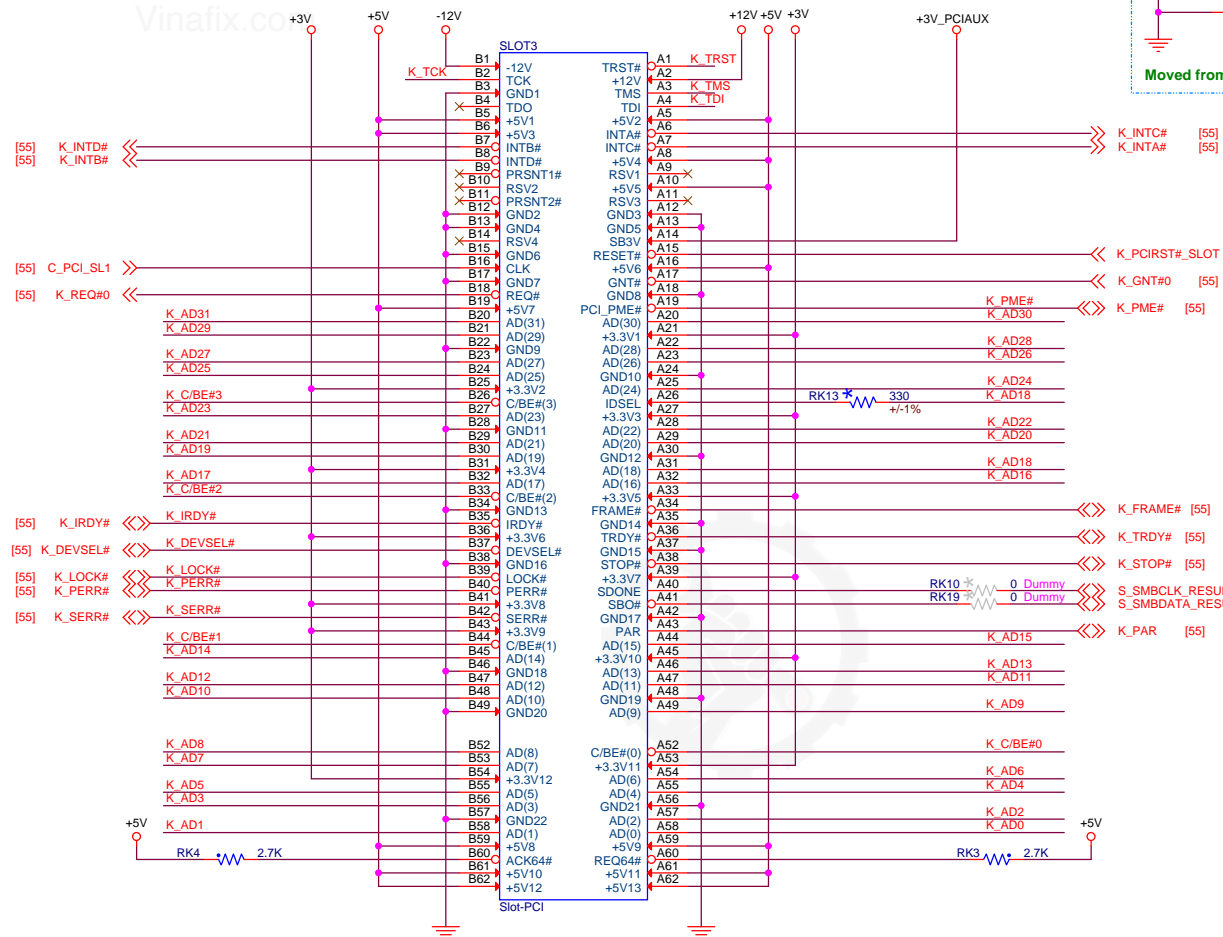


If used PCH GPIO13 PCIE RESET Mode:  
Stuffed RX21 => all PCIe w/o PEG  
Stuffed RX22 => all PCIe w/ PEG





IRQ: CDAB  
IDSEL: AD18  
REQ/GNT: 0



Title

## PCI Slot

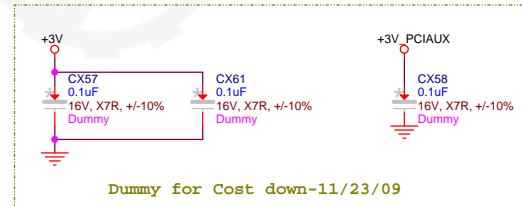
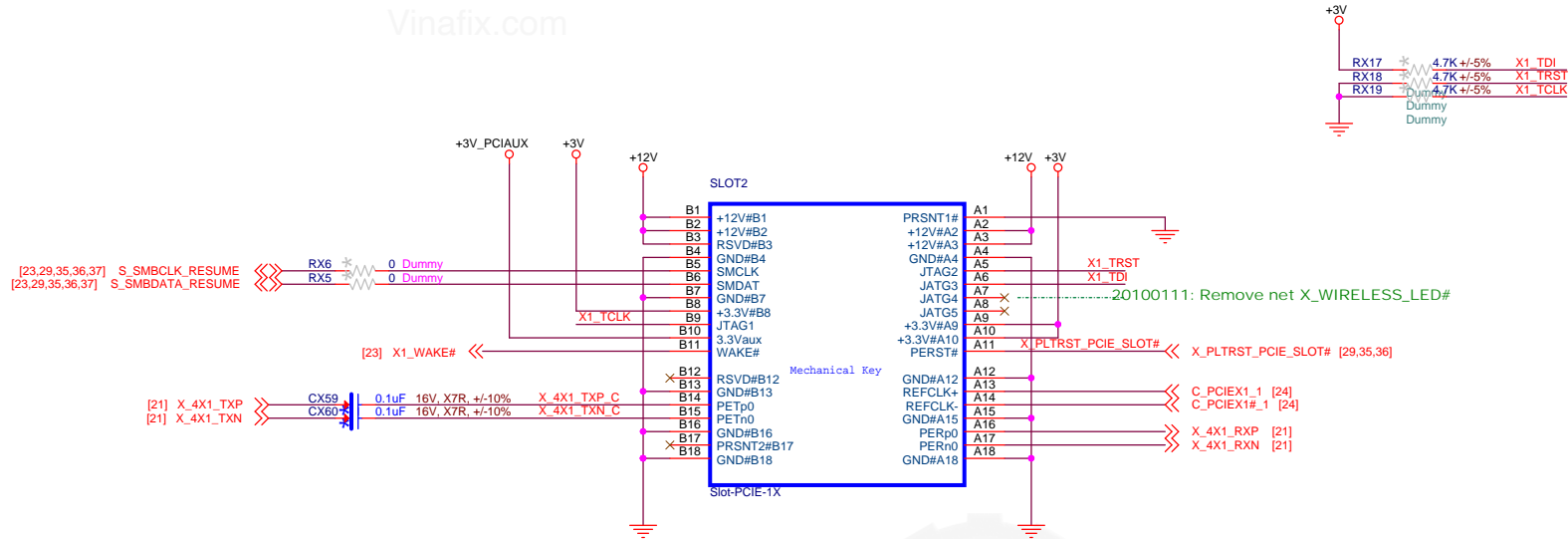
DWG NO
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Title

PCIe 1x

DWG NO

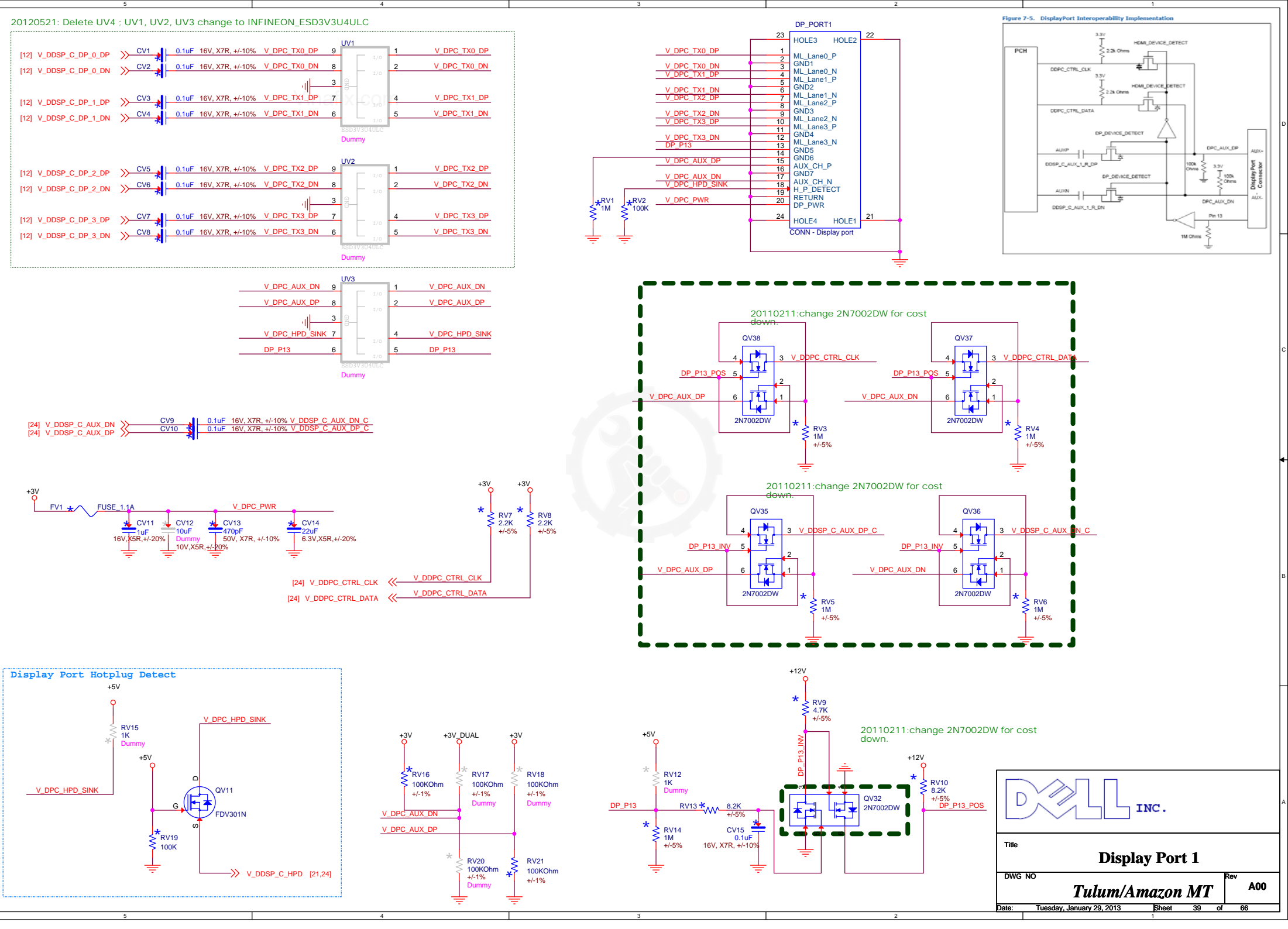
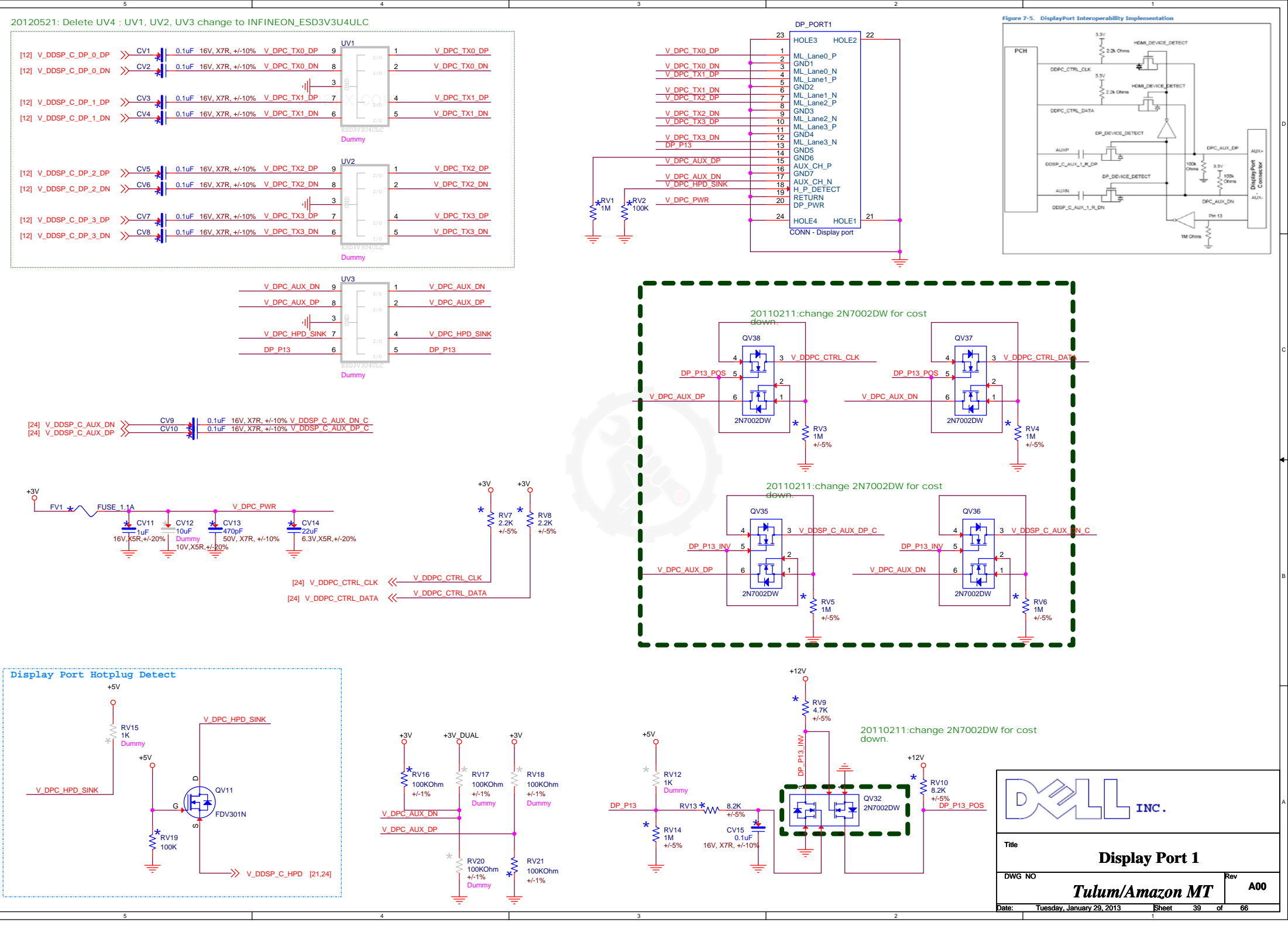
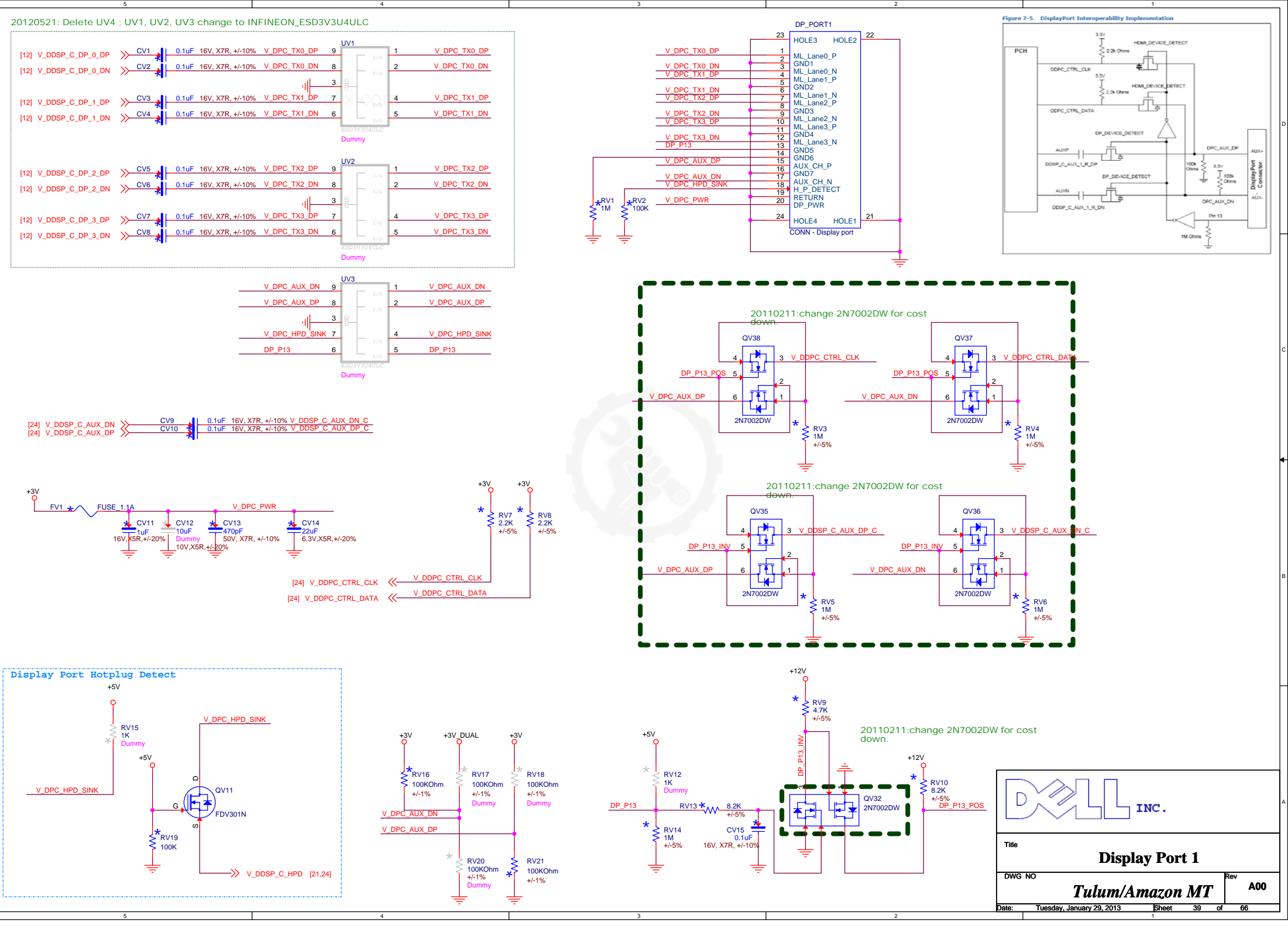
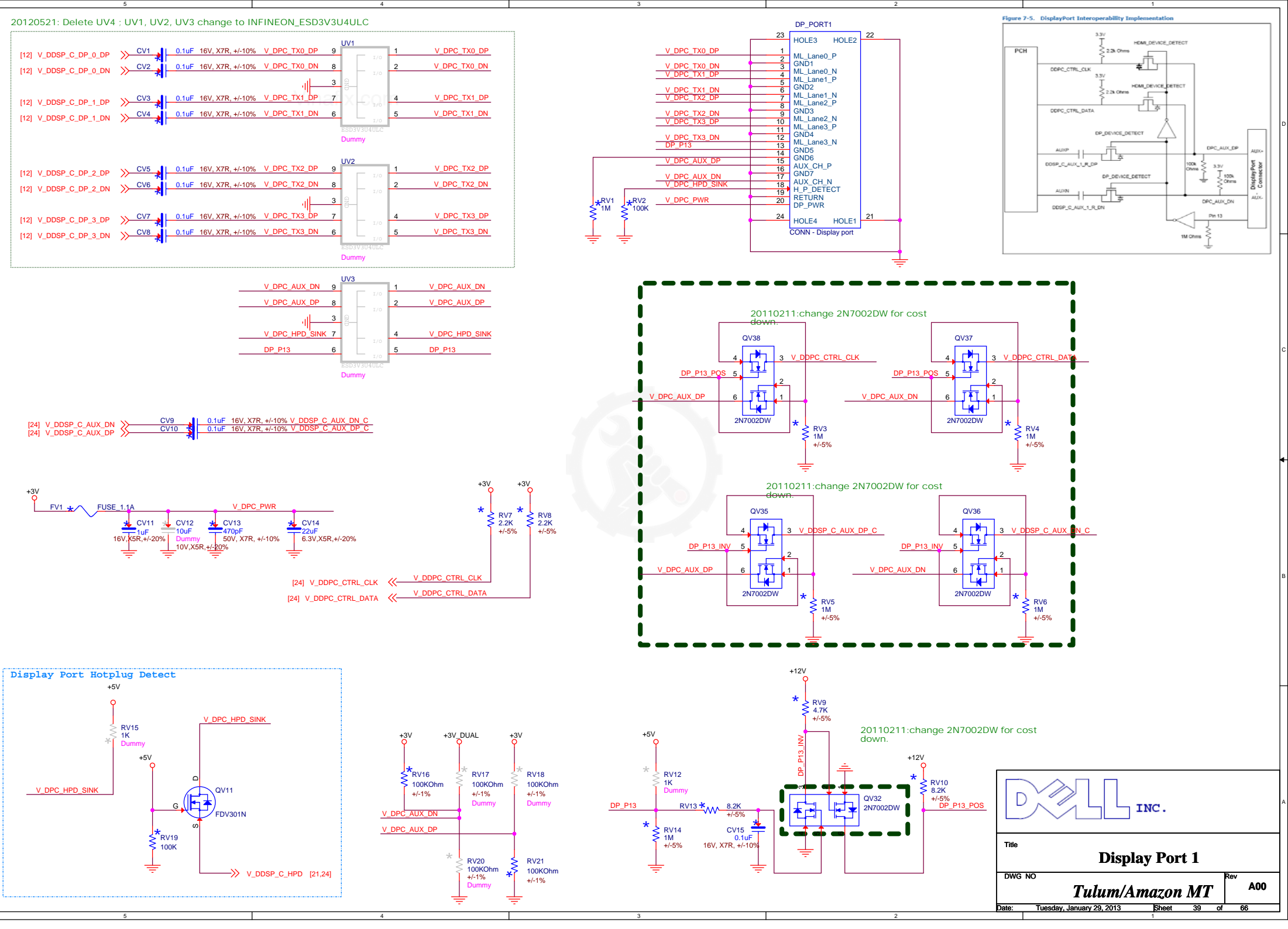
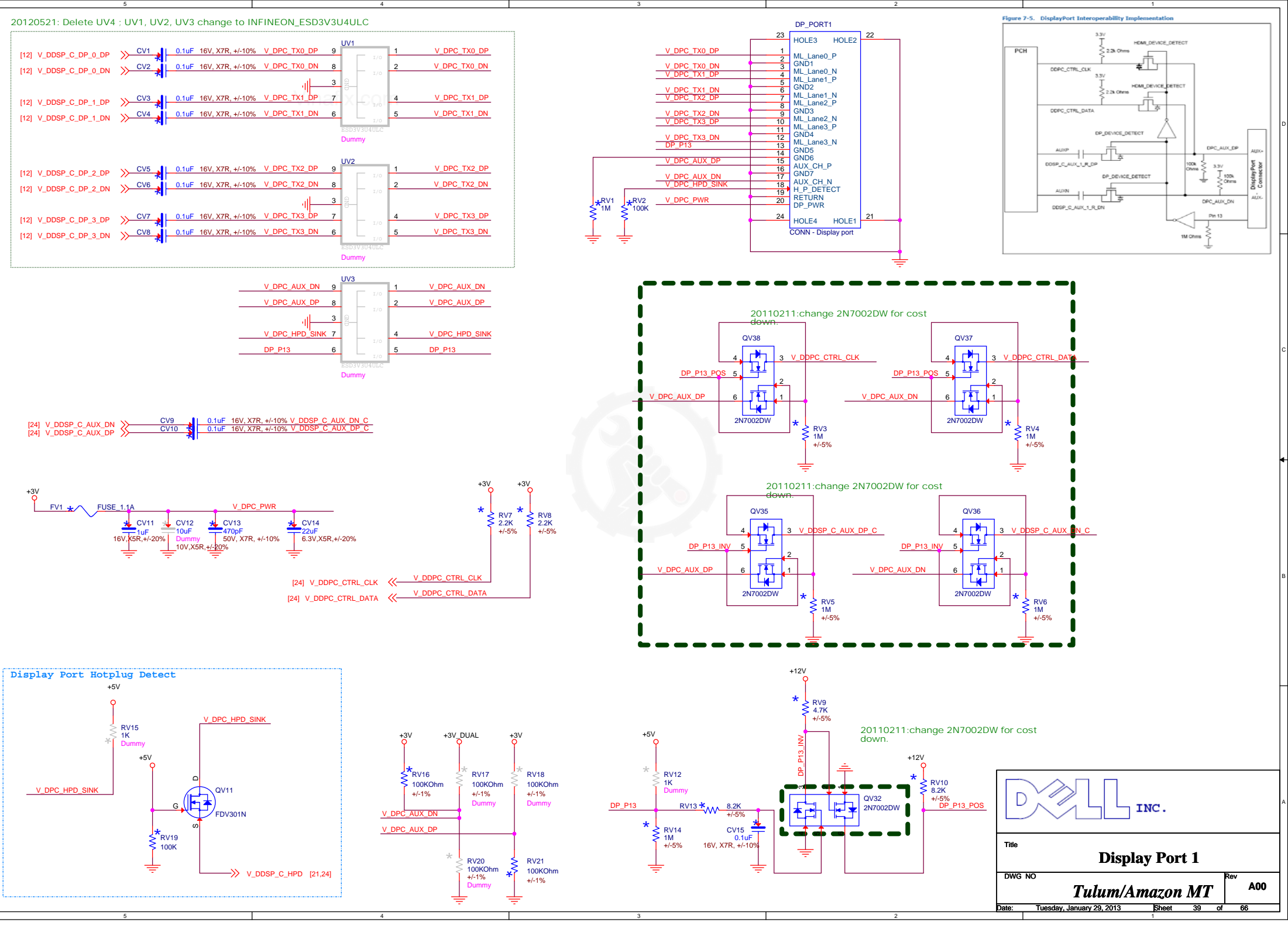
Tulum/Amazon MT

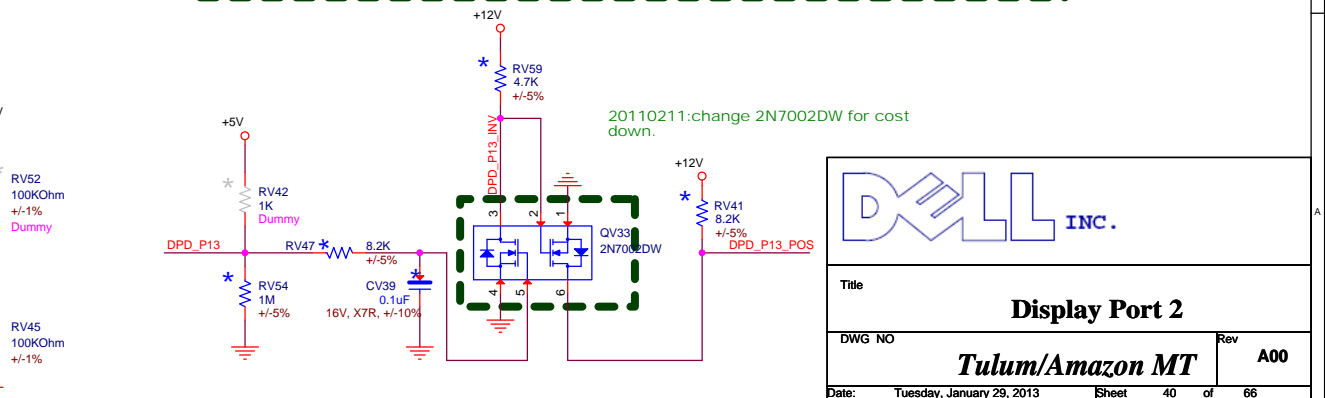
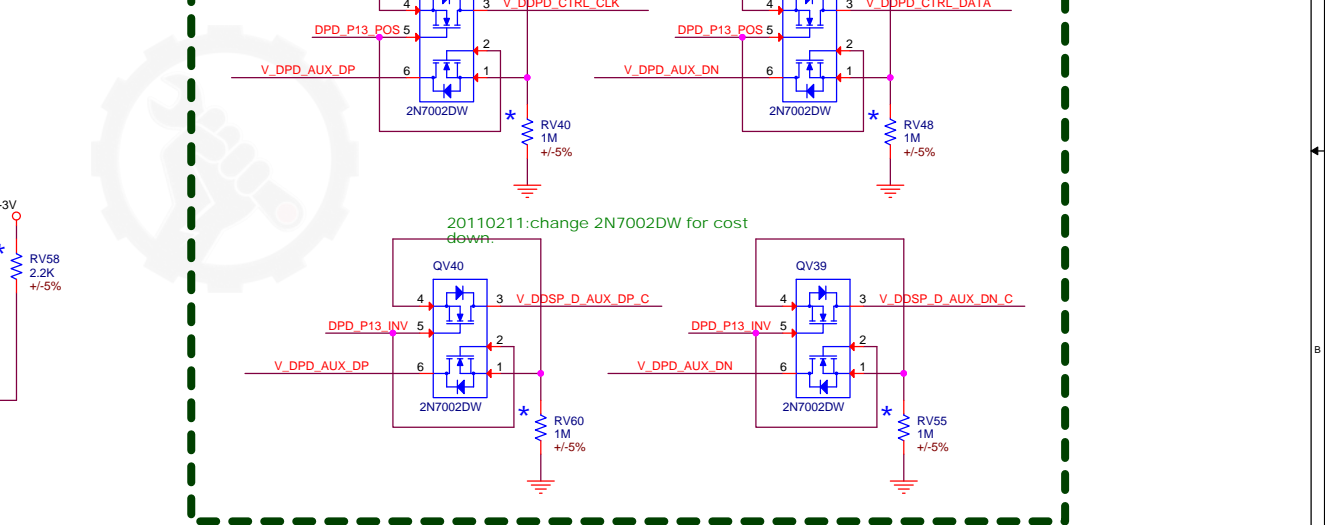
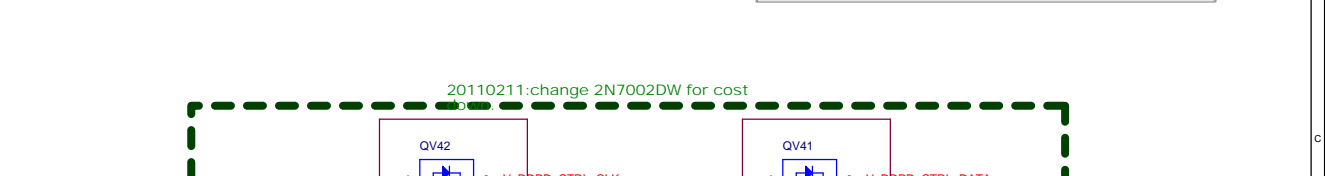
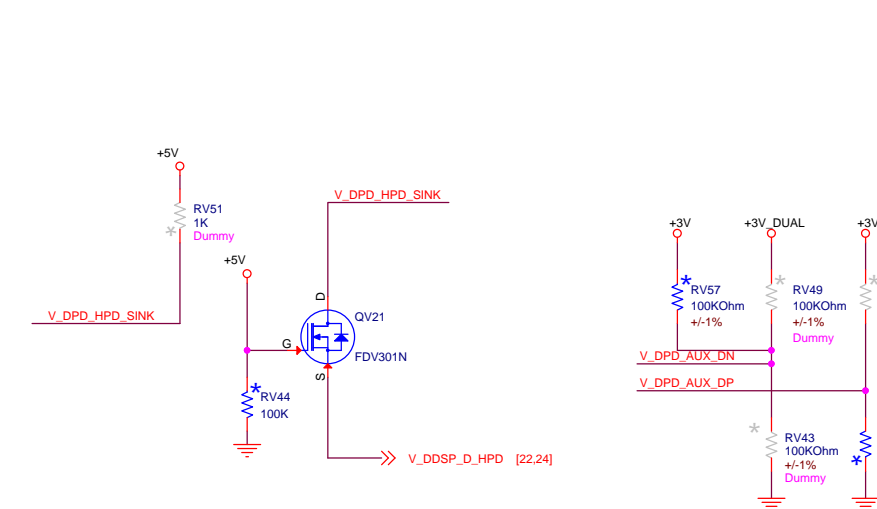
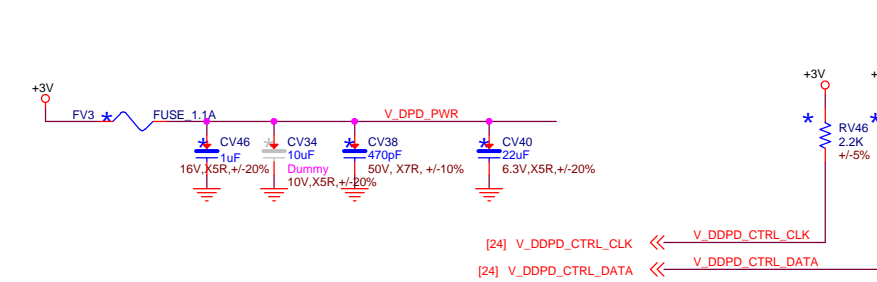
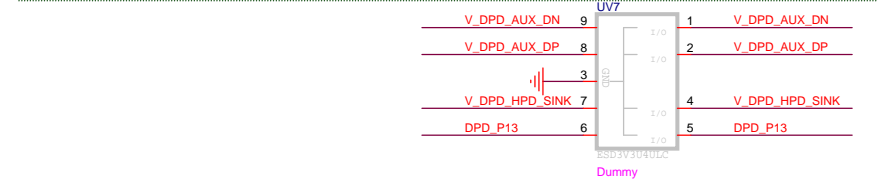
Rev

A00

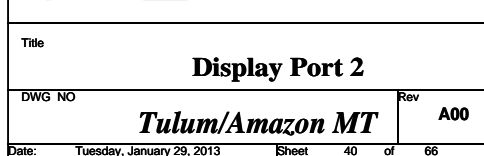
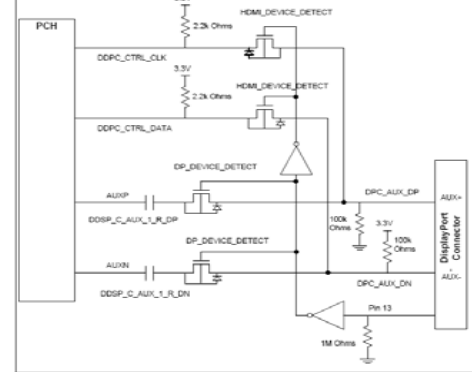
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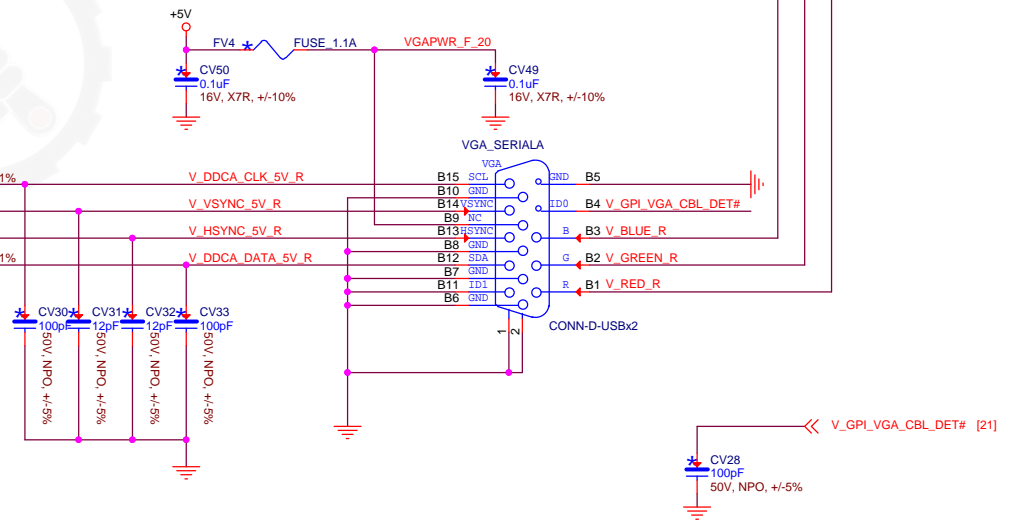
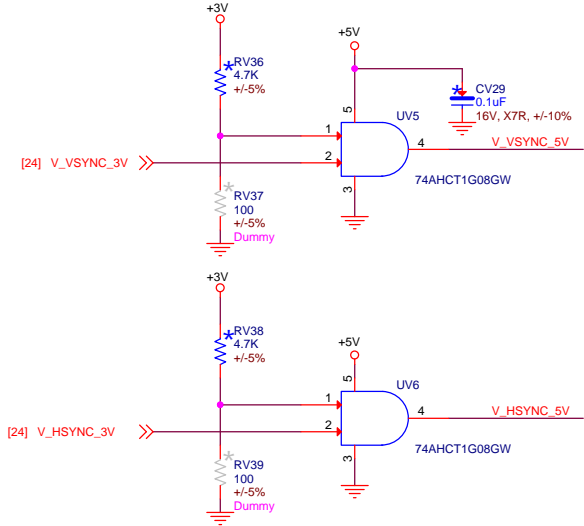
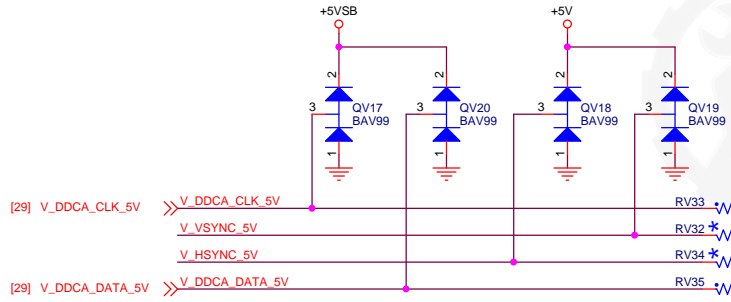
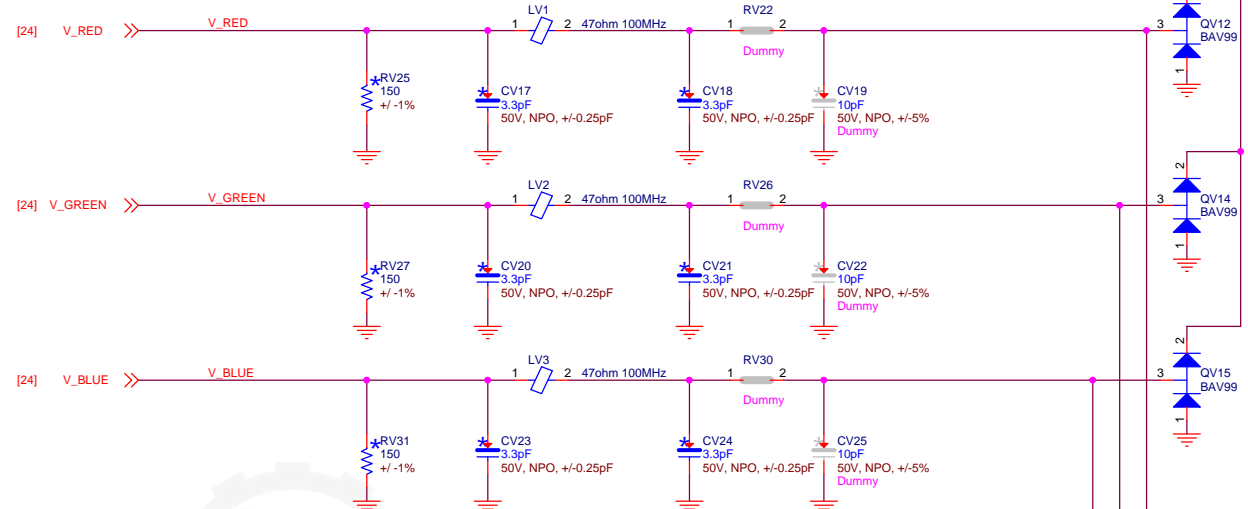
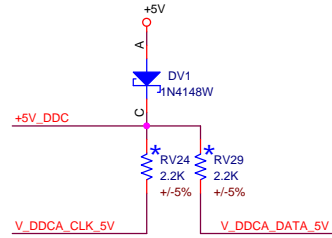


	3.304
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# VGA Connector

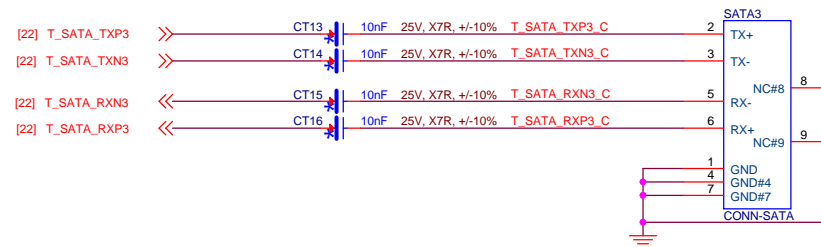
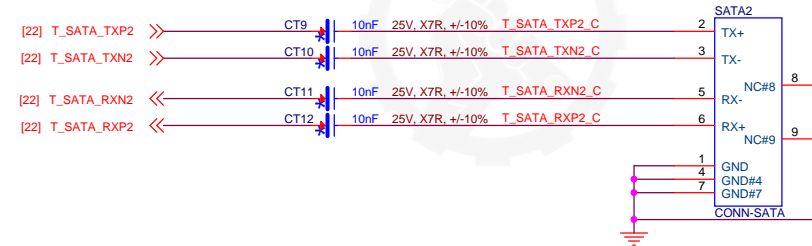
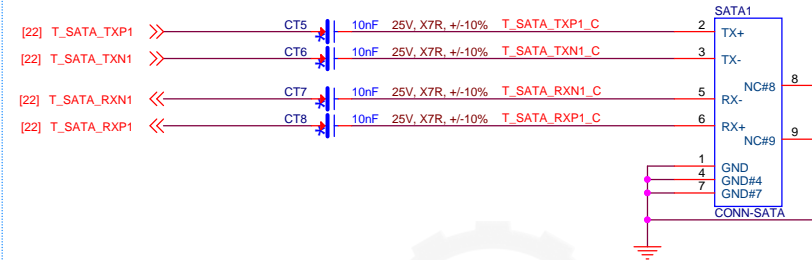
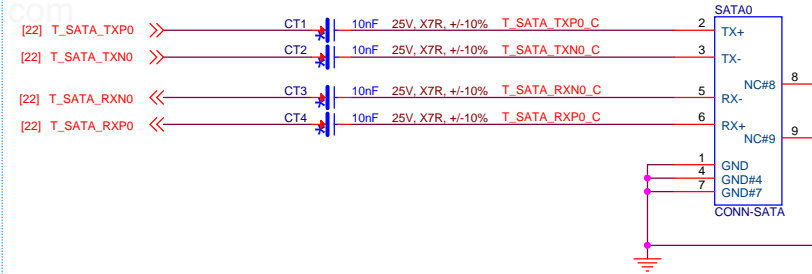
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Title		
VGA Conn		
DWG NO	Tulum/Amazon MT	Rev A00
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# SATA Gen.3

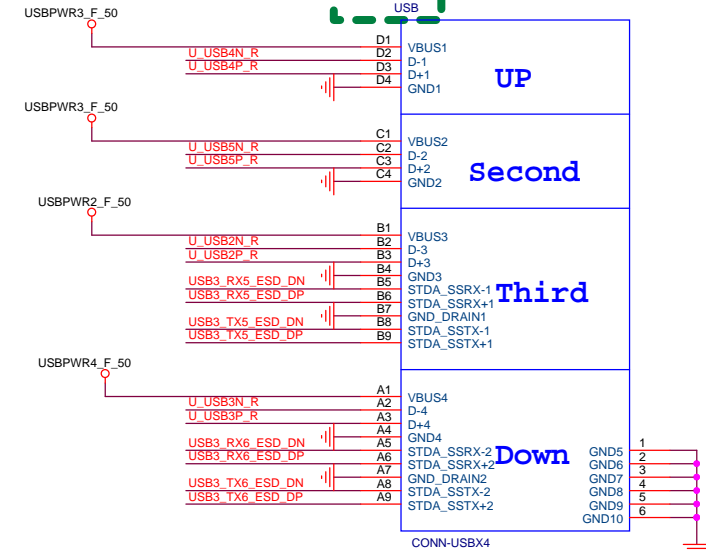
Vinafix.com



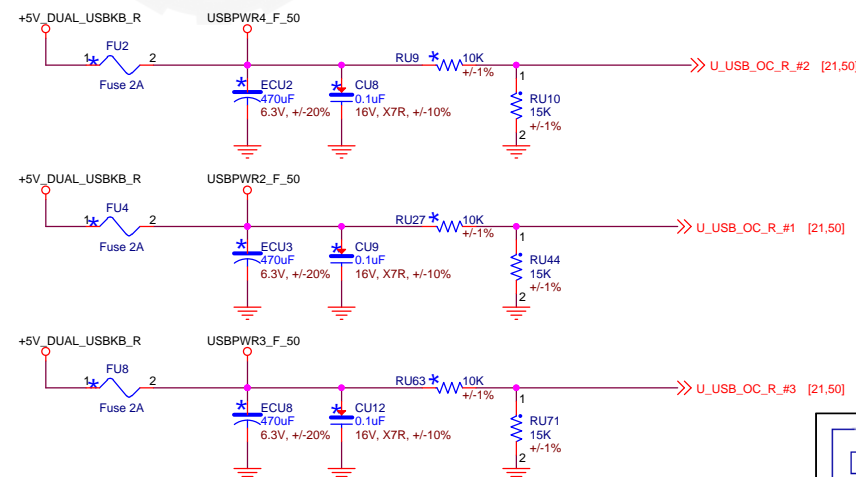
Title		
SATA Conn		
DWG NO	Tulum/Amazon MT	Rev A00
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# Rear USB CONNECTOR

20120214: USB change to Black USB3.0 CONN



Place ESD Close to Connector

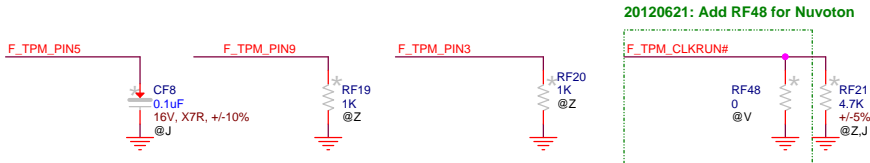
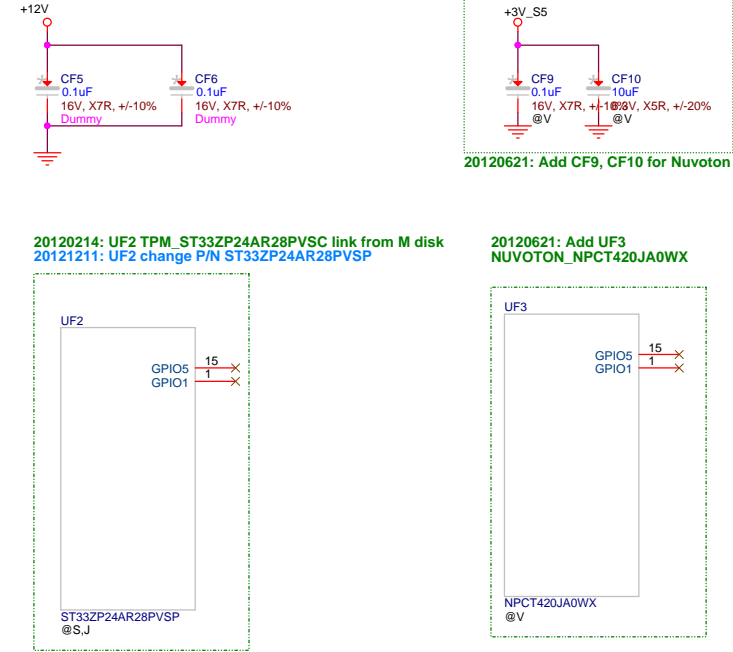
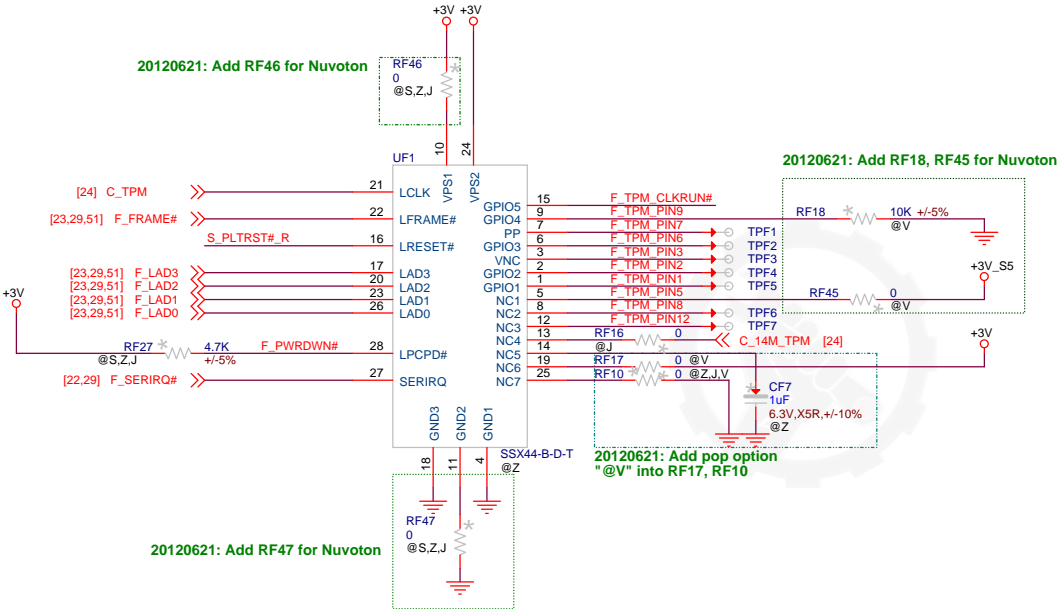
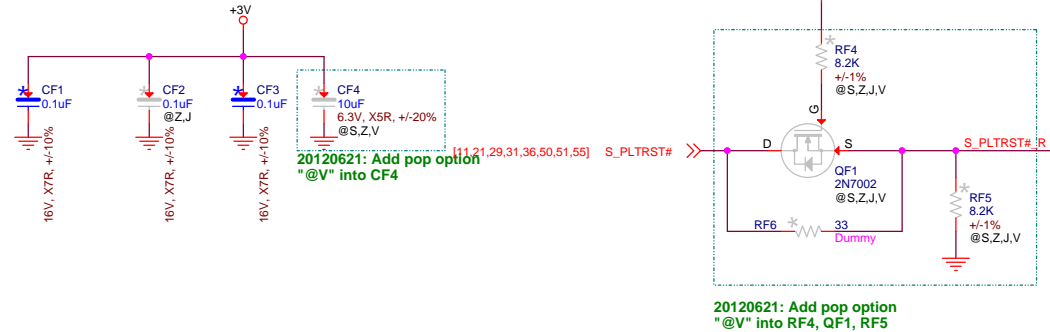


Title		
Rear USB		
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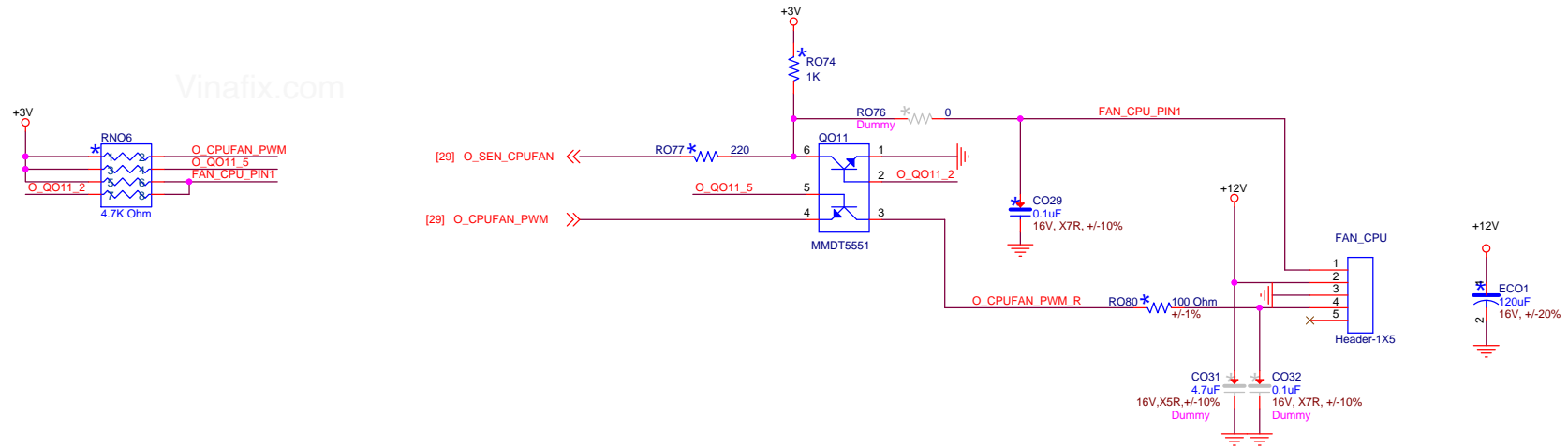


TPM, TCM (TCM is just reserved because MRD has removed TCM requirement)

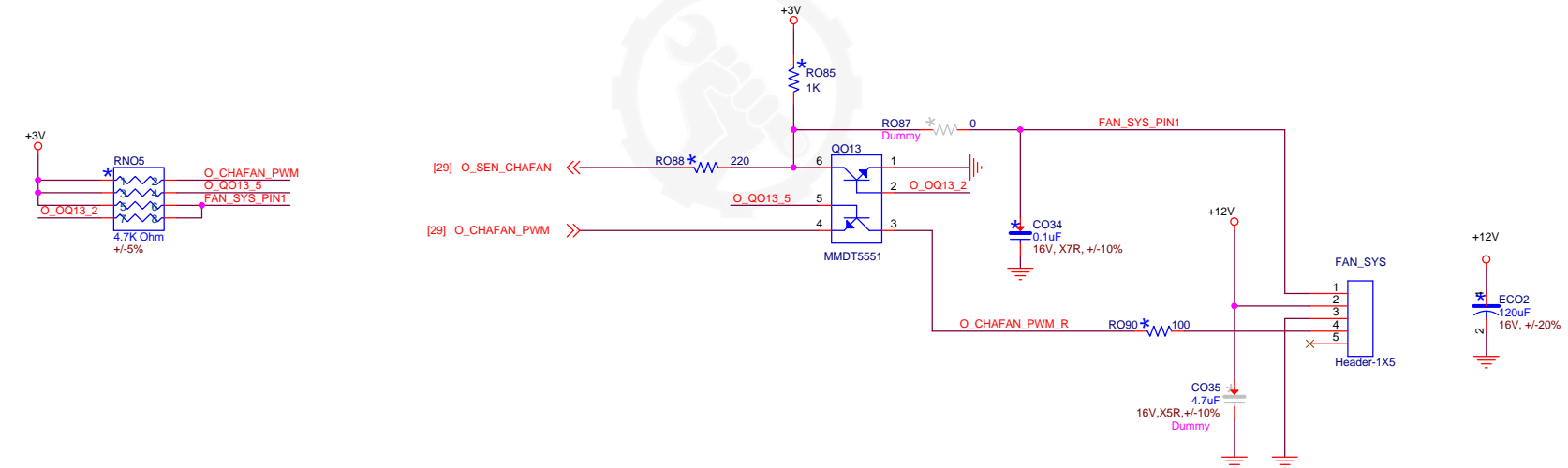
(Default) ST Micro	POP S	CF4,RF4,RF5,QF1,RF46,RF27,RF47
ZTE	POP Z	RF4,RF5,QF1,RF46,RF27,CF2,CF4,CF7,RF47,RF10,RF19,RF20,RF21
Jetway	POP J	CF2,CF8,RF10,RF16,RF21,RF47,RF27,RF46,RF4,RF5,QF1
Nuvelton	POP V	CF9,CF10,CF4,RF18,RF45,RF17,RF10,RF48,RF4,RF5,QF1



CPU Fan



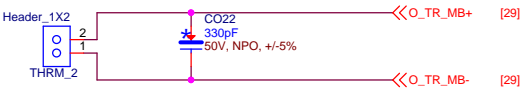
SYS Fan



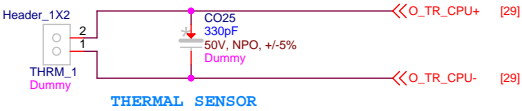
PSU Fan




Title			FAN		
DWG NO			Tulum/Amazon MT		
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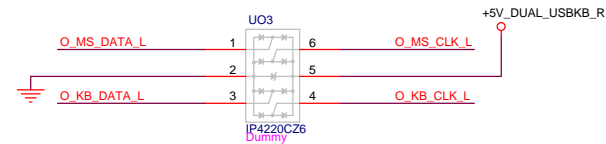
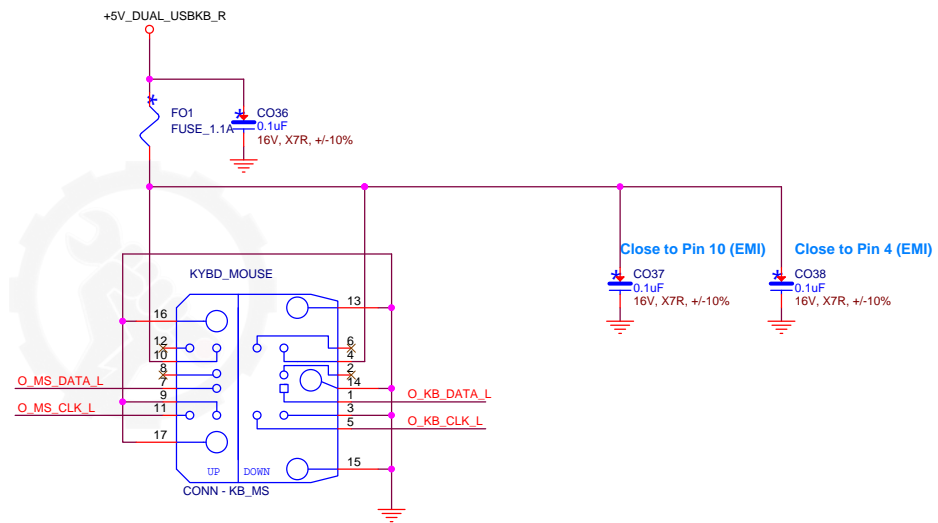
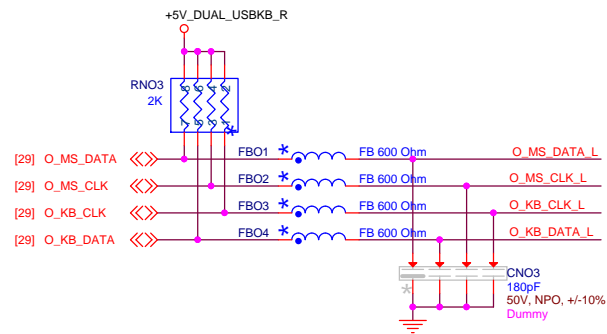
Dummy THRM2,CO23; ME suggestion-12/04/09





INC.

Title	
Thermal Sensor	
DWG NO	Rev
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Title

PS2 Conn

DWG NO

Tulum/Amazon MT

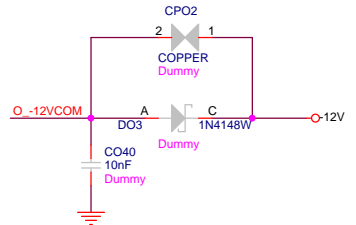
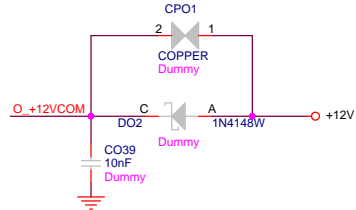
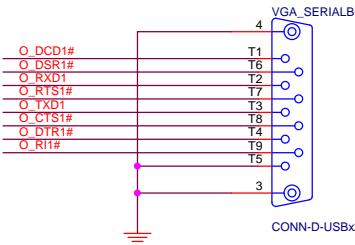
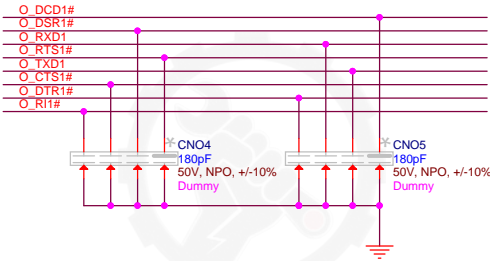
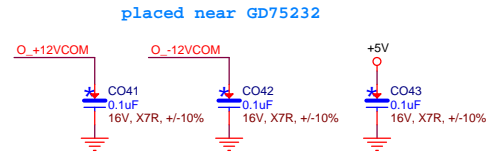
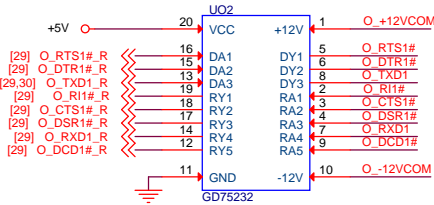
Rev  
A00

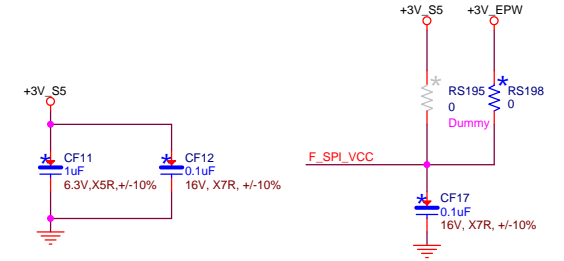
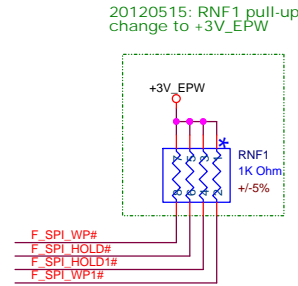
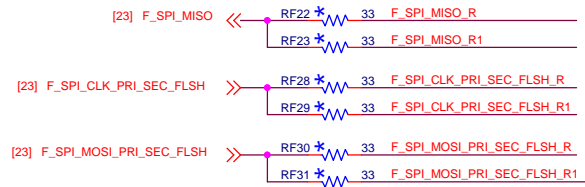
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Serial Port 1

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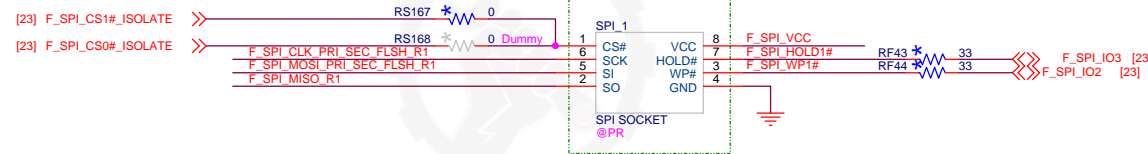
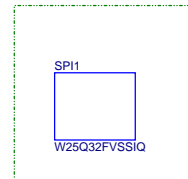




## SPI\_4MB

20110530: SPI1 Change to 4M

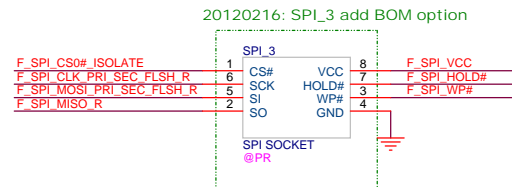
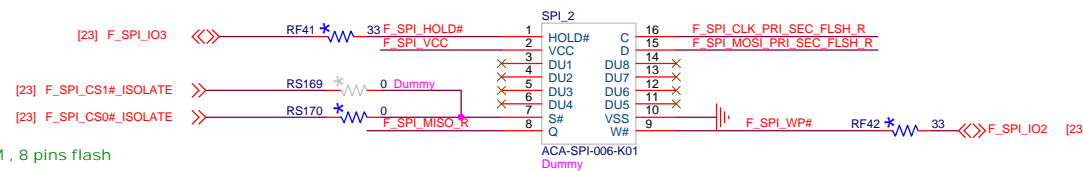
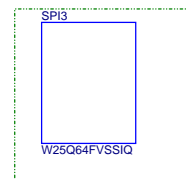
20120216: SPI1 Change to WINBOND\_W25Q32BVSSIG



## SPI\_8MB

20120216: SPI2 rename to SPI3 and Change to 8M , 8 pins flash

20120216: SPI3 and Change to 8M , 8 pins flash, WINBOND\_W25Q64FVSSIG

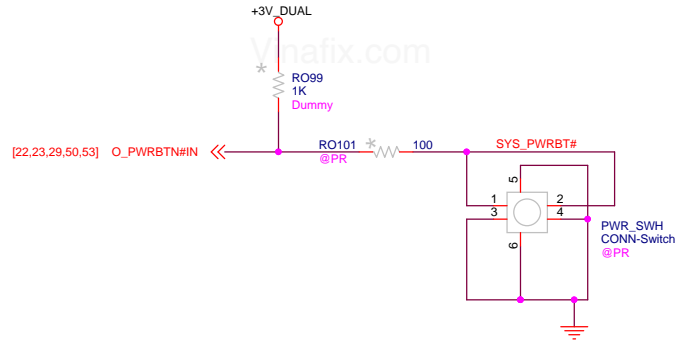


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SPI	
DWG NO	Rev
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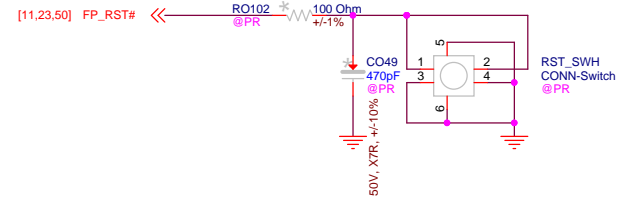




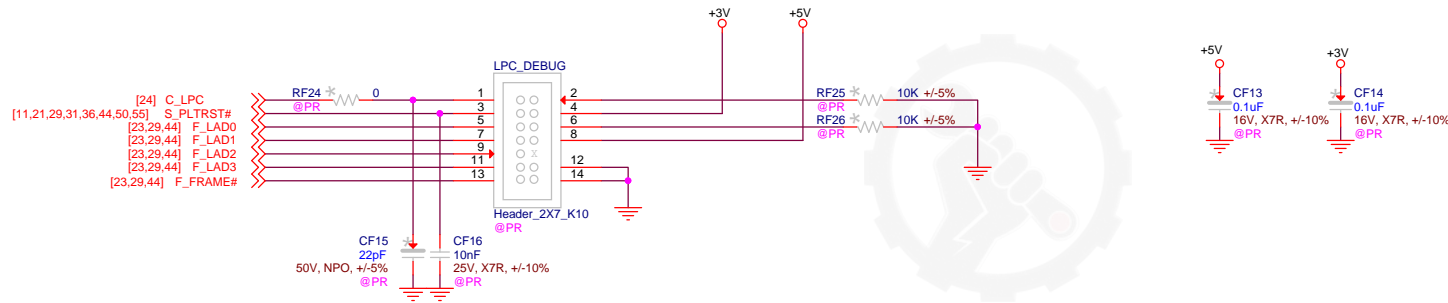
## Power Bottom



## Reset Bottom



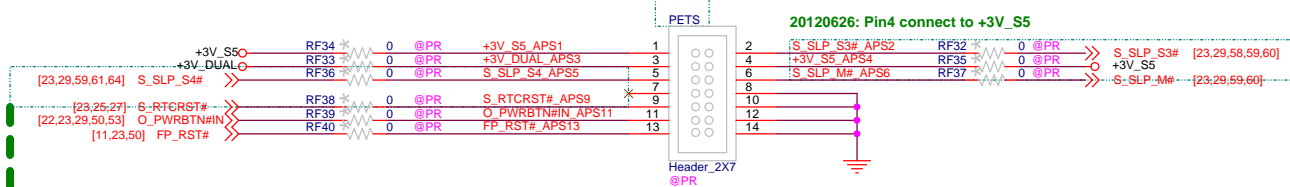
## LPC DEBUG



## APS Debug

20120621: rename to PETS

20120626: Pin4 connect to +3V\_S5

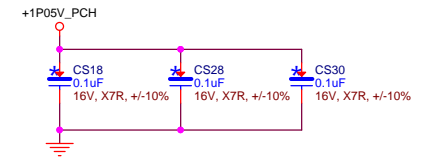
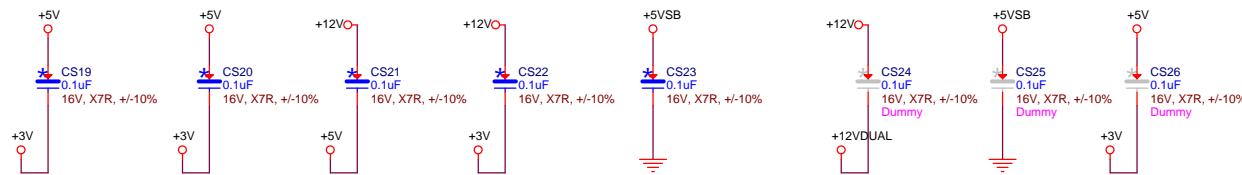
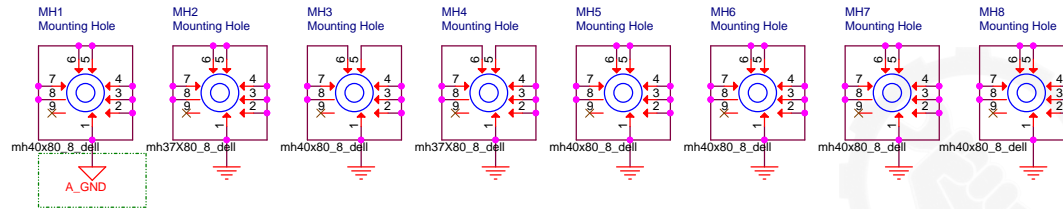
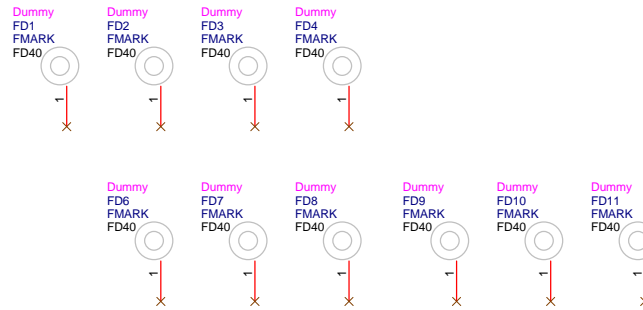
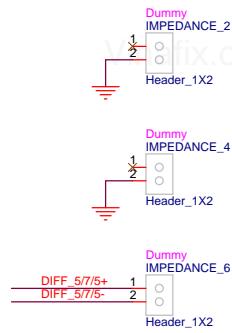
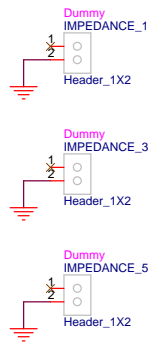


20120626: Pin7 net rename to +3V\_DUAL\_APS7 and add RF49 connect to +3V\_DUAL

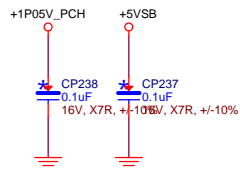
20120626: Pin7 let NC

Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7		Unused
Pin 8	GND	Ground
Pin 9	RTCSRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCSRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

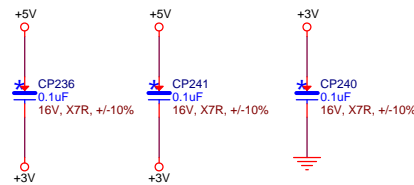




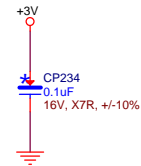
for H\_ITPCLK.



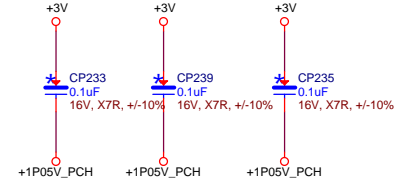
for C\_PCI\_SB.



for A\_Z\_Bitclk.



for Front USB3.0

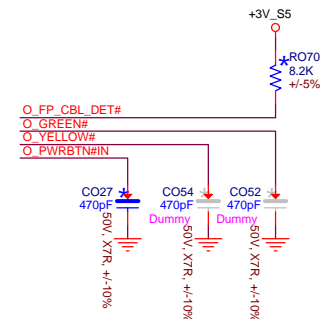
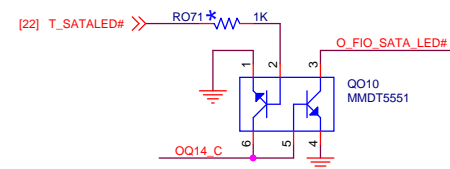
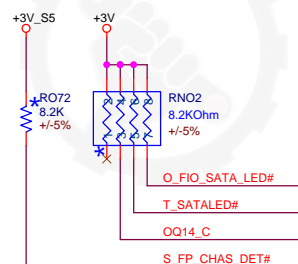
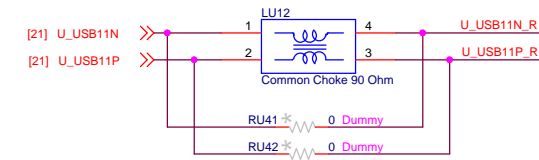
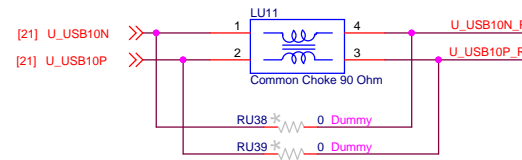
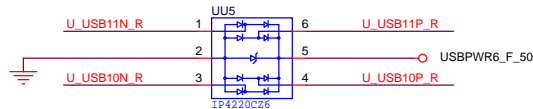
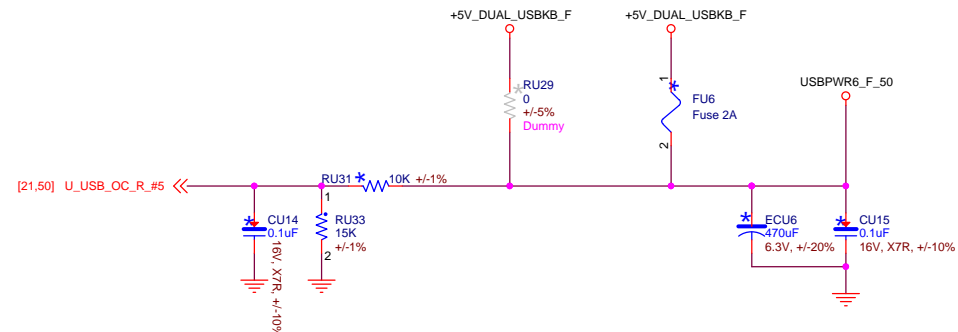
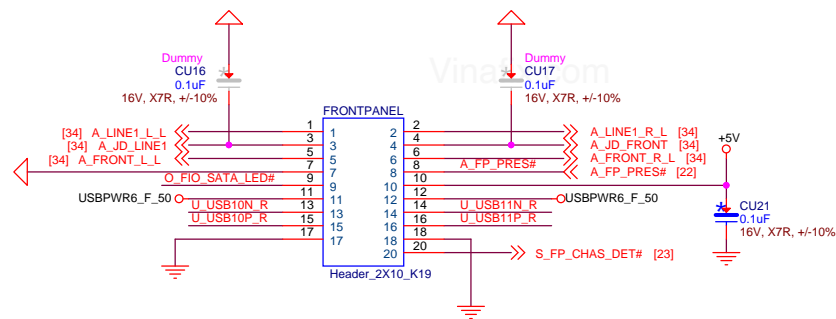


**EMI**

DWG NO **Tulum/Amazon MT** Rev **A00**

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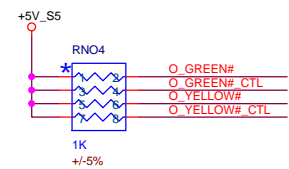
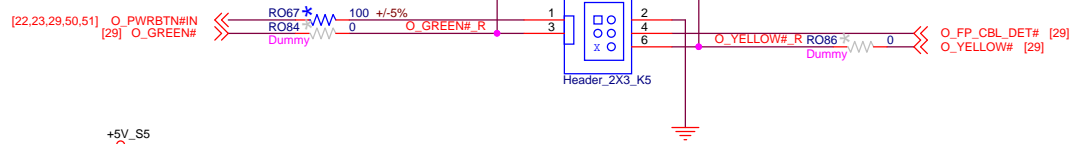
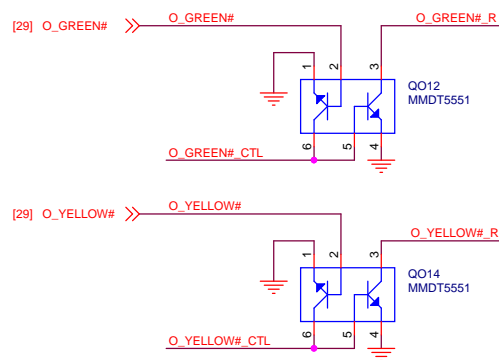
# Front USB/LED Header




## POWER SWITCH Header

20120521: Add QO12, QO14, RNO4, RO84, RO86 for Power LED control

If stuffed RO84, RO86 ; Dummy QO12, QO14, RNO4





Title

DWG NO

Date: Tuesday, January 29, 2013

**Front\_Panel**

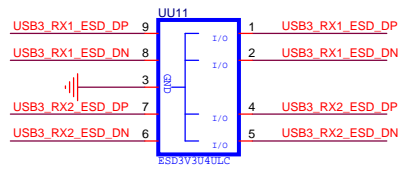
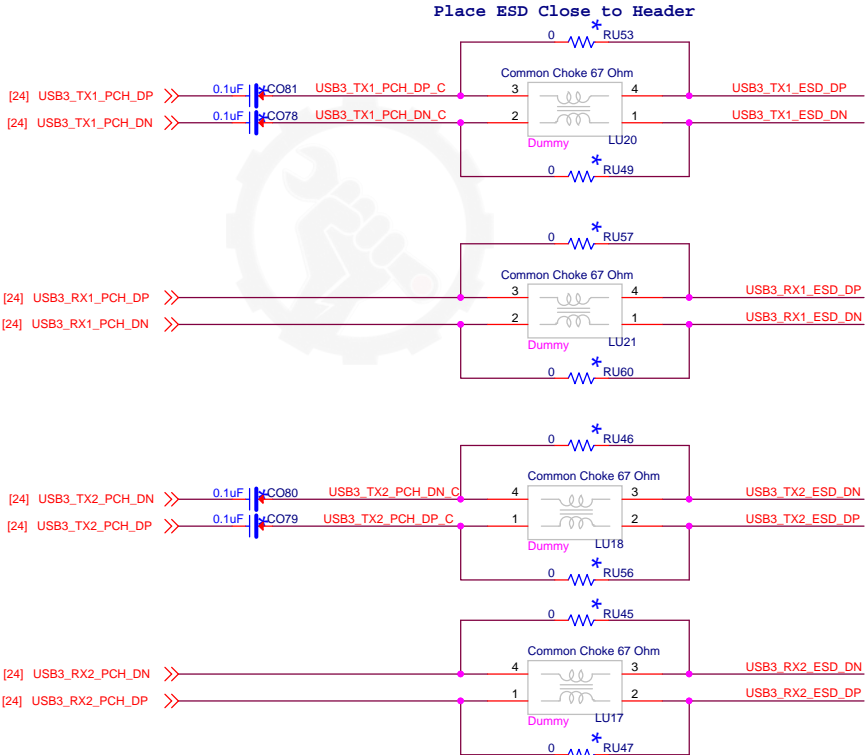
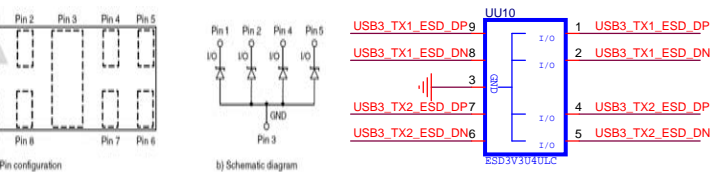
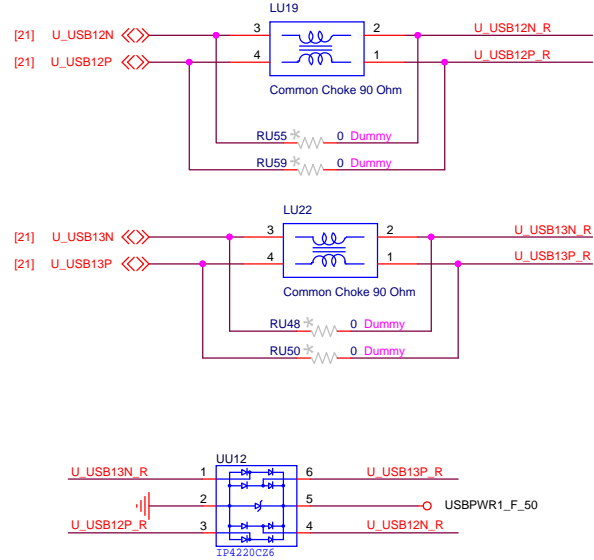
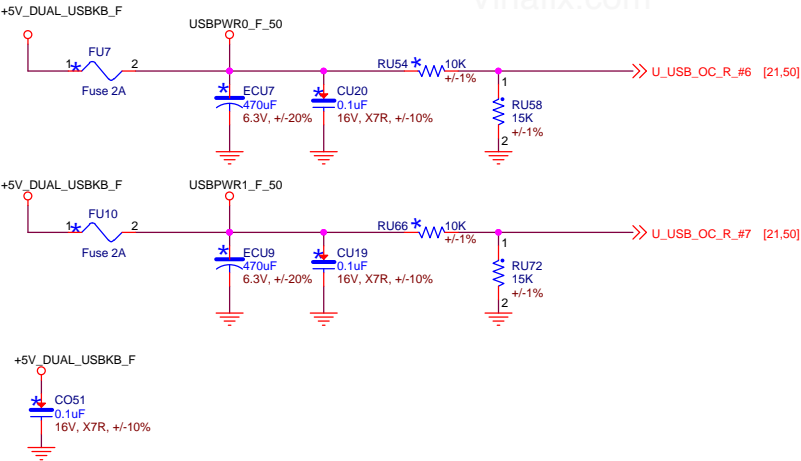
**Tulum/Amazon MT**

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Front USB/LED Header



2012014: USB3\_FRONT connector change to PUB200-2017-B5-10-HF.

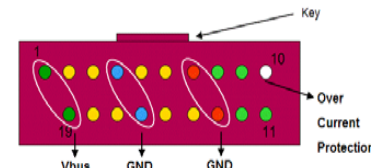
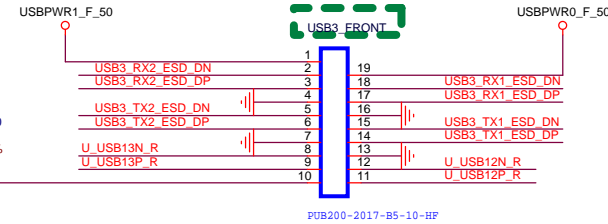
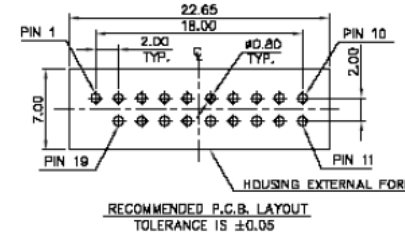
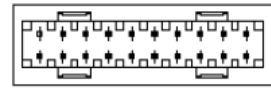


Figure 2-1: USB3 ICC pin numbering



Title

TBD

DWG NO

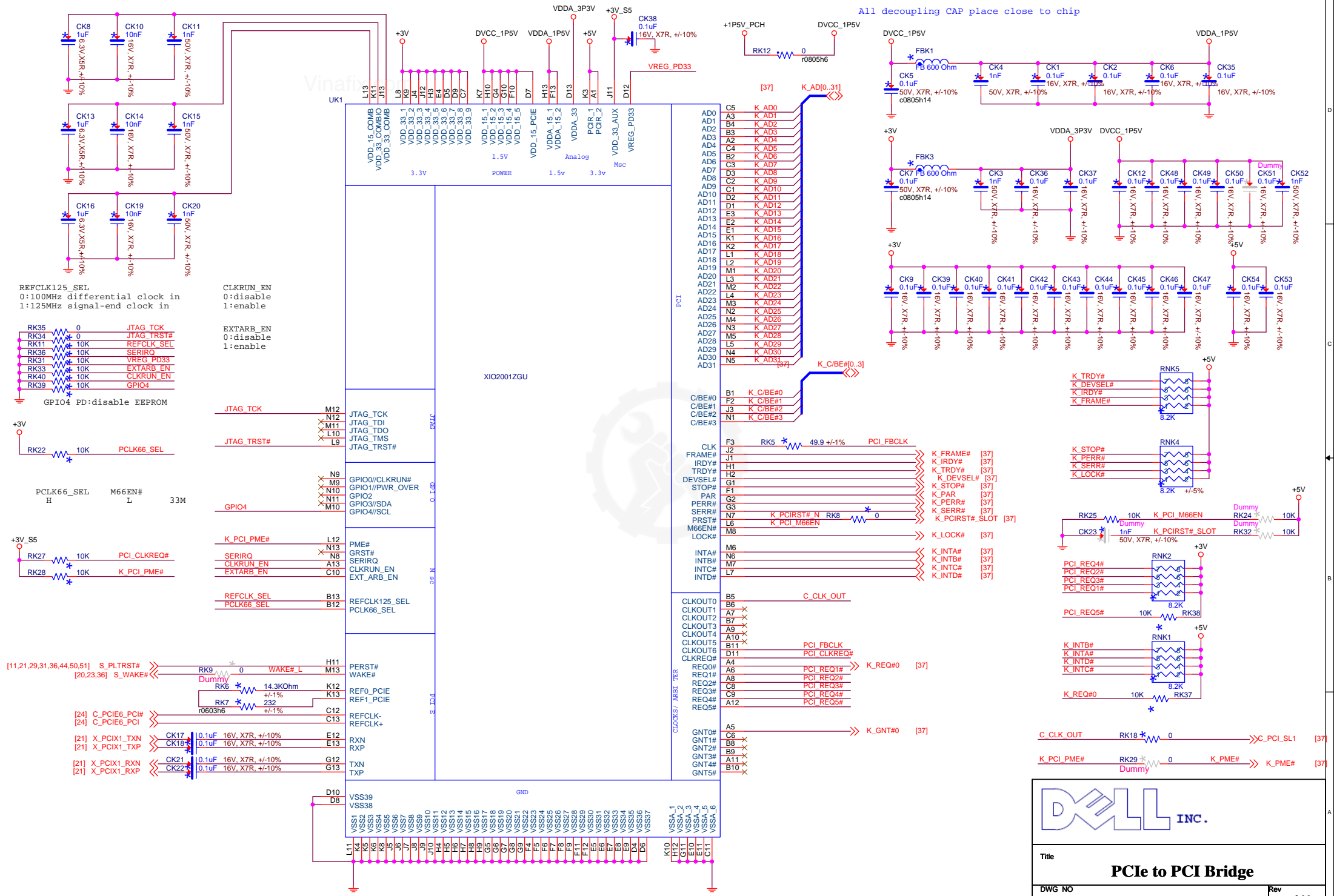
Tulum/Amazon MT

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Rev

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Title

**PCIe to PCI Bridge**

DWG NO

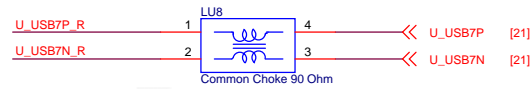
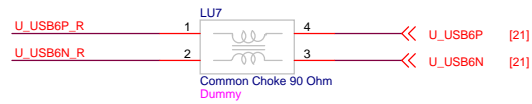
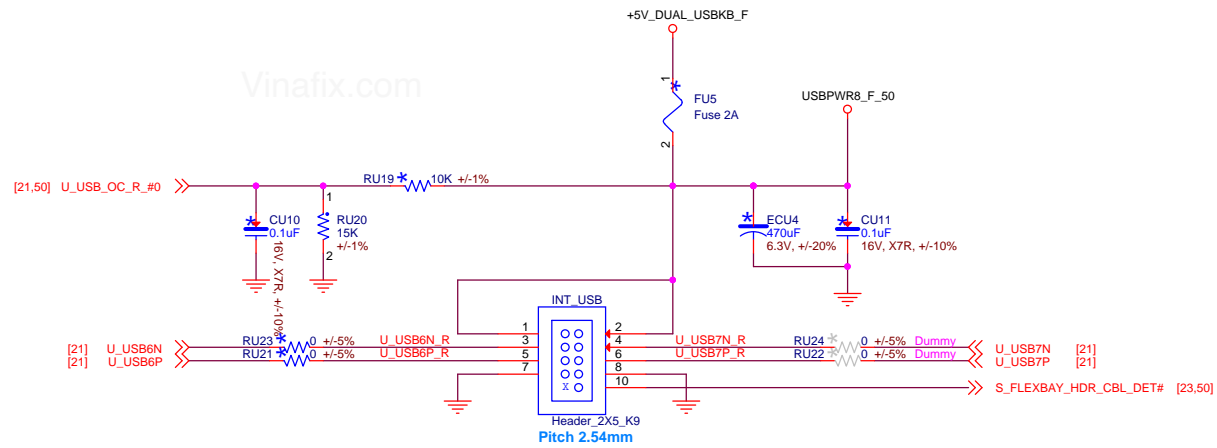
**Tulum/Amazon MT**

Date: Tuesday, January 29, 2013

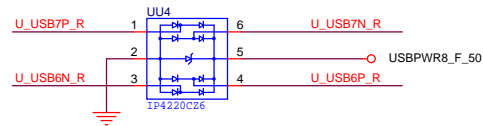
Rev

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CO-LAY with 4 Serial resistors RU21, RU22, RU23, & RU24



Title

**Internal USB**

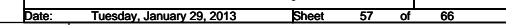
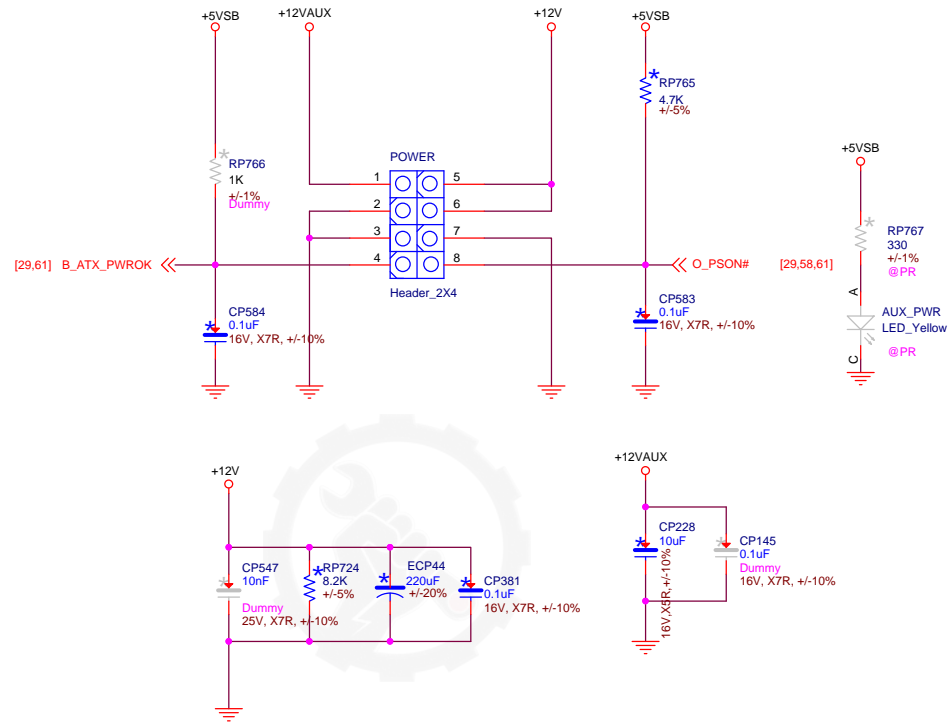
DWG NO

**Tulum/Amazon MT**

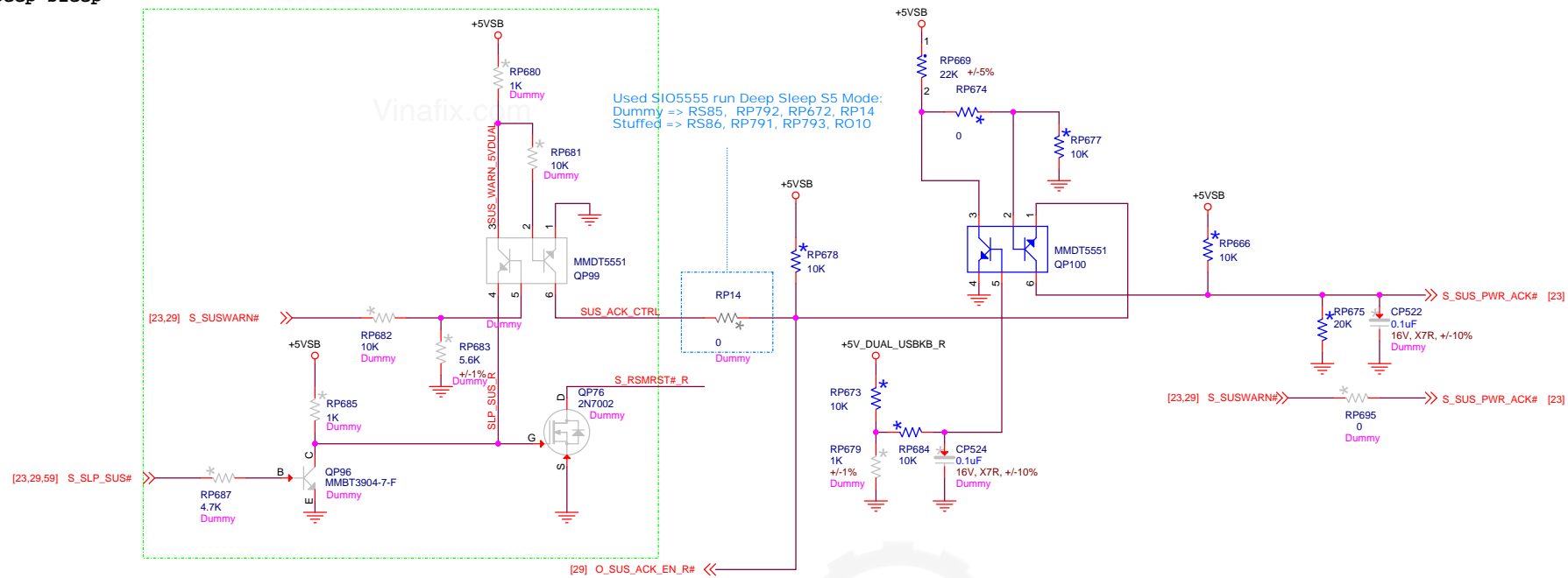
Rev **A00**

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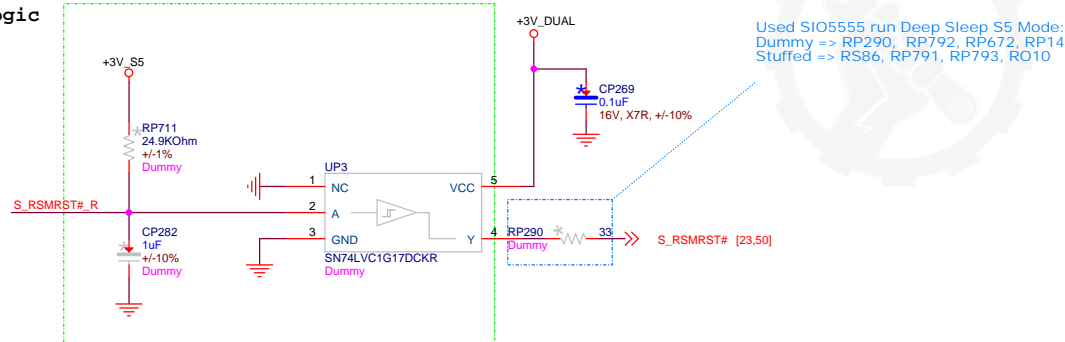
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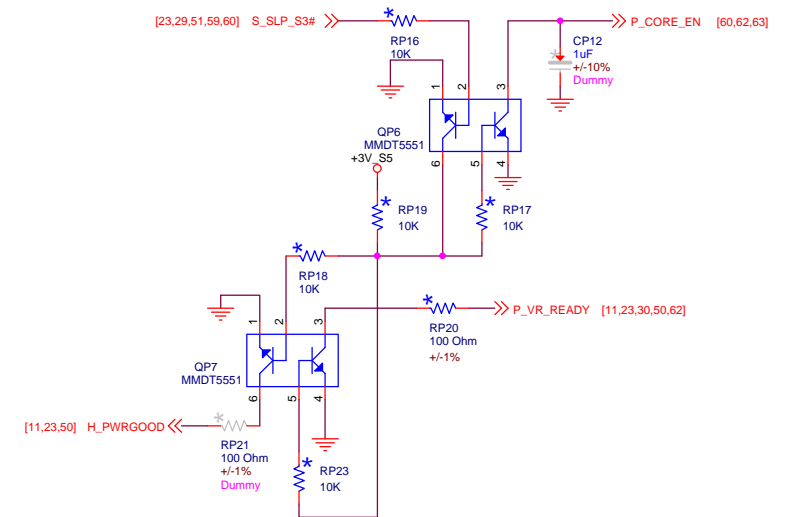
## For Deep Sleep



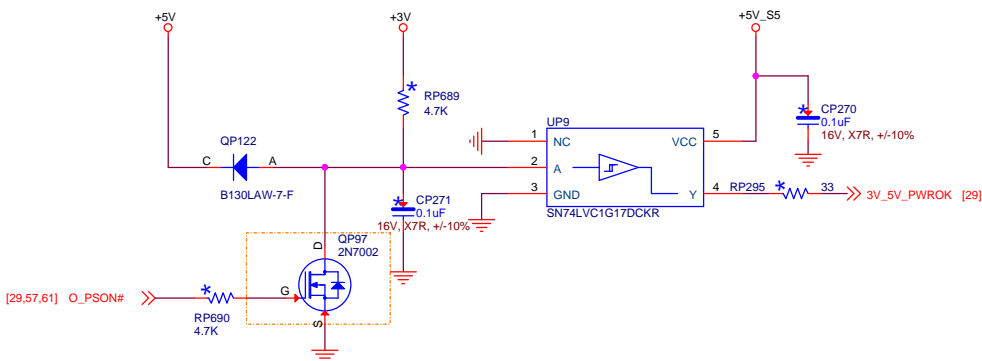
## RESUME RESET Logic



## VR\_READY DEFENSIVE



## New ATXPWROK

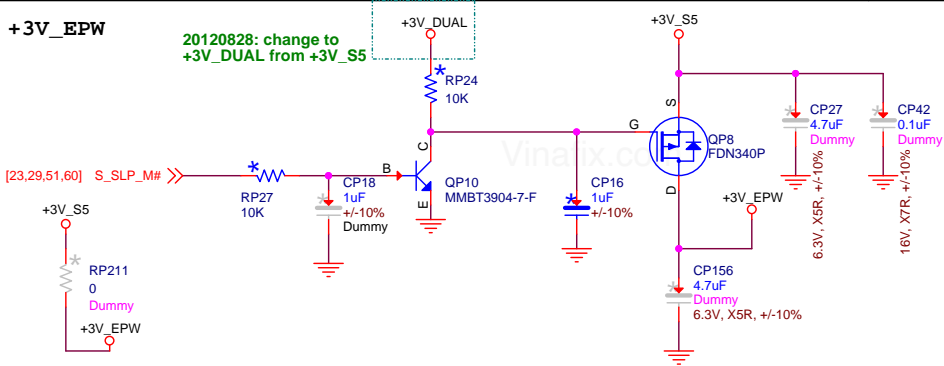


Title		
Power Sequence		
DWG NO	Tulum/Amazon MT	Rev A00
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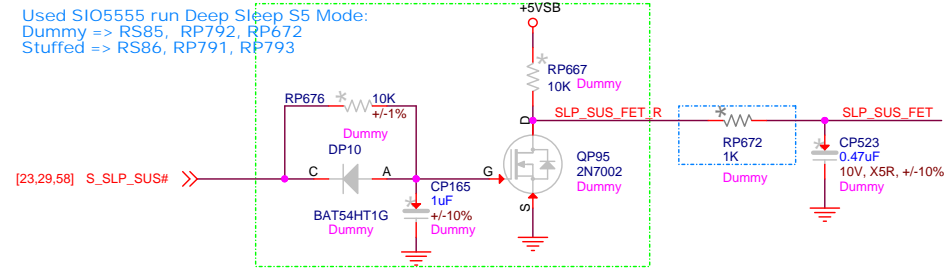


### +3V\_EPW

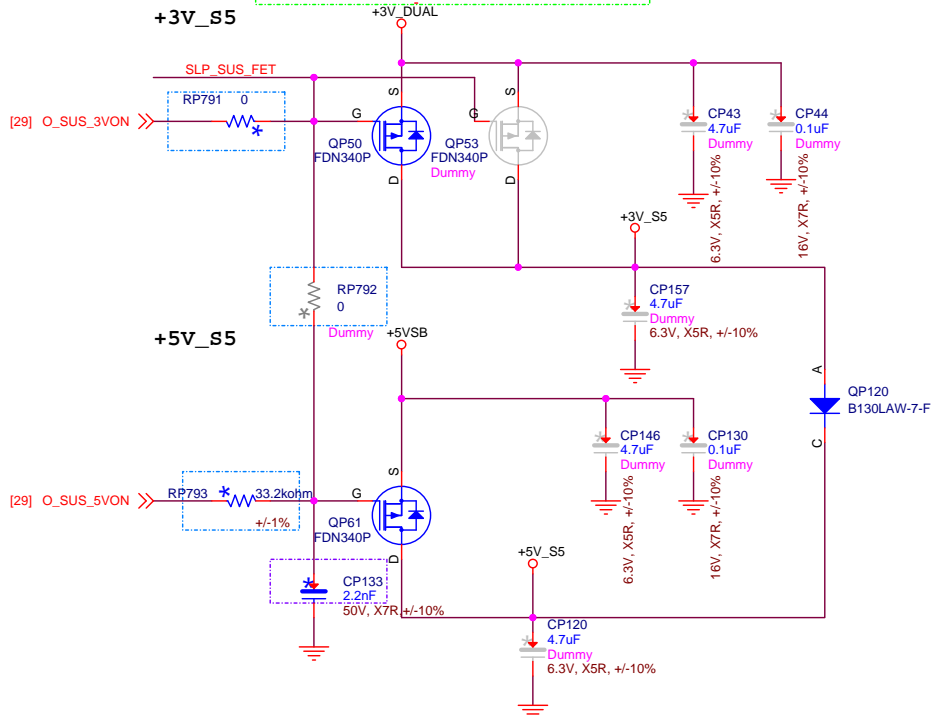
20120828: change to  
+3V\_DUAL from +3V\_S5



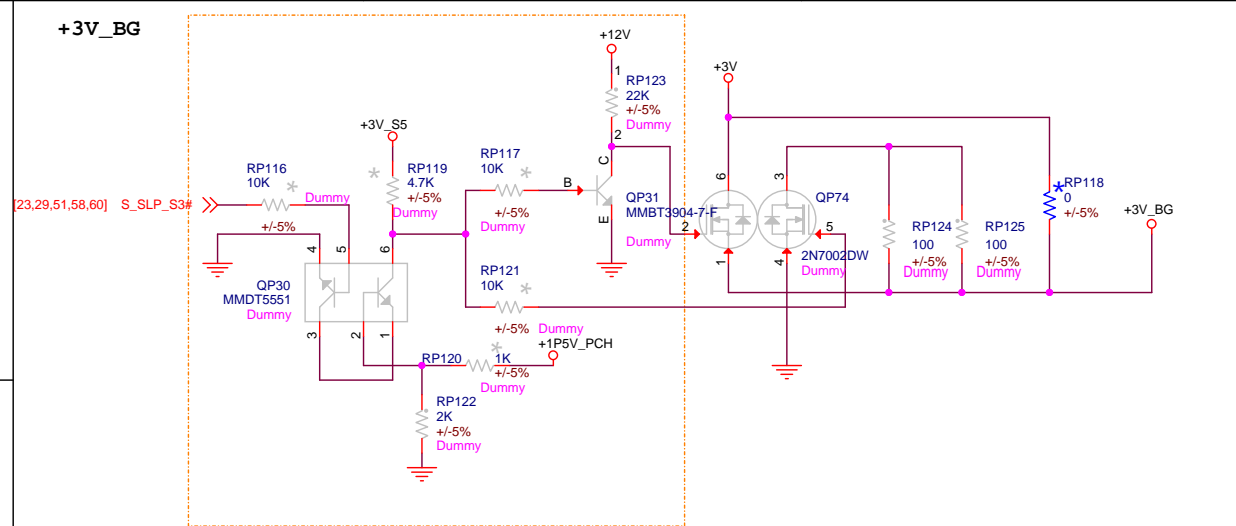
Used SIO5555 run Deep Sleep S5 Mode:  
Dummy => RS85, RP792, RP672  
Stuffed => RS86, RP791, RP793



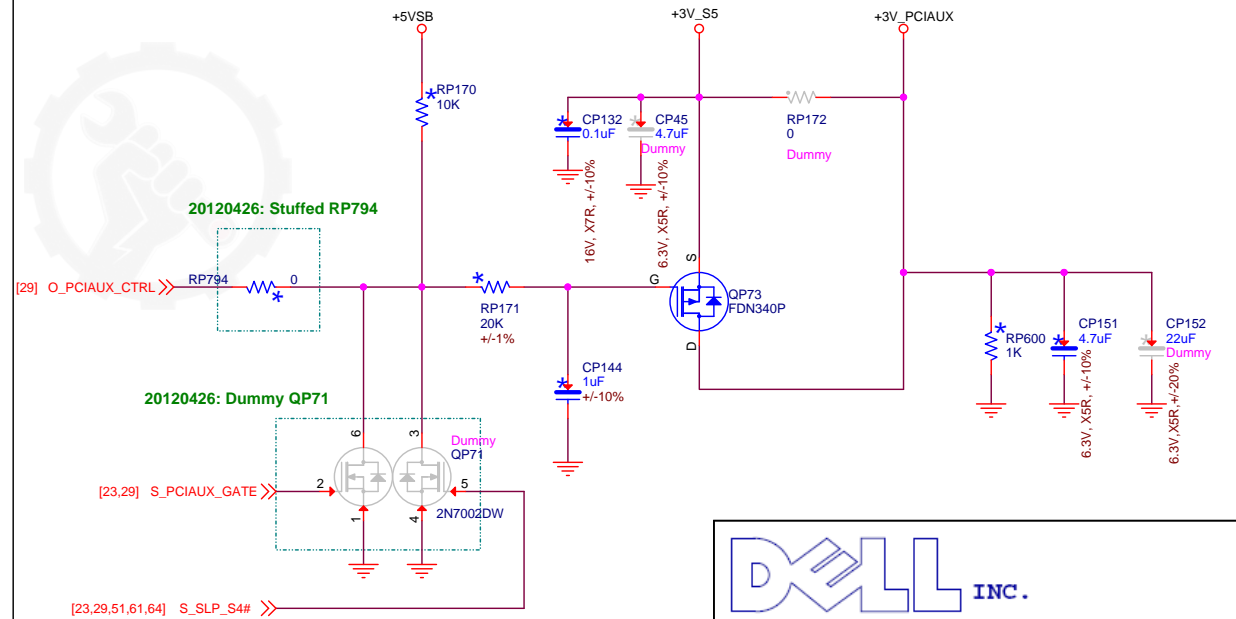
### +3V\_S5



### +3V\_BG

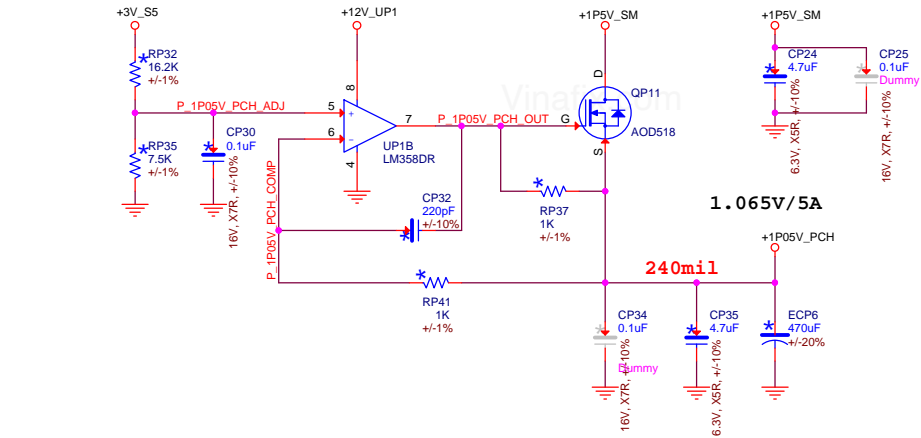


### +3V\_PCIAUX(FOR PCI/PCIE SLOT)

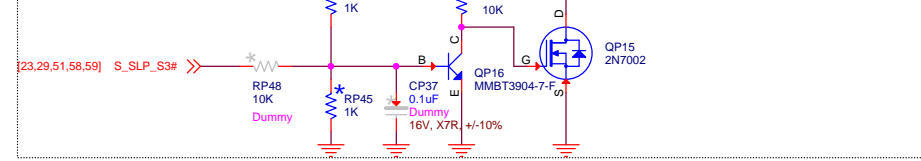


Title		
Power-1:Linear Power-1		
DWG NO	Tulum/Amazon MT	Rev A00
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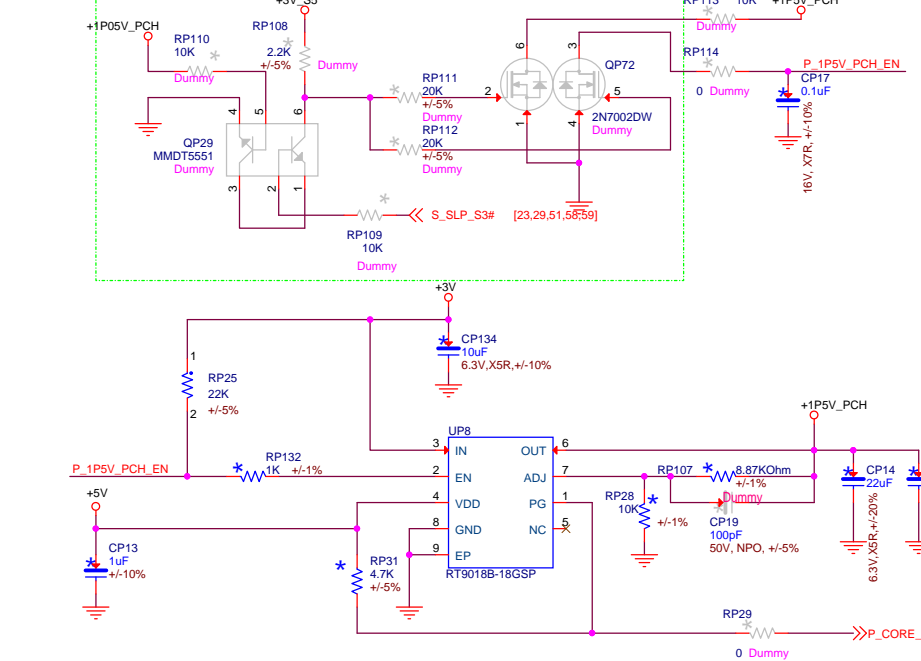
+V\_1.05\_PCH



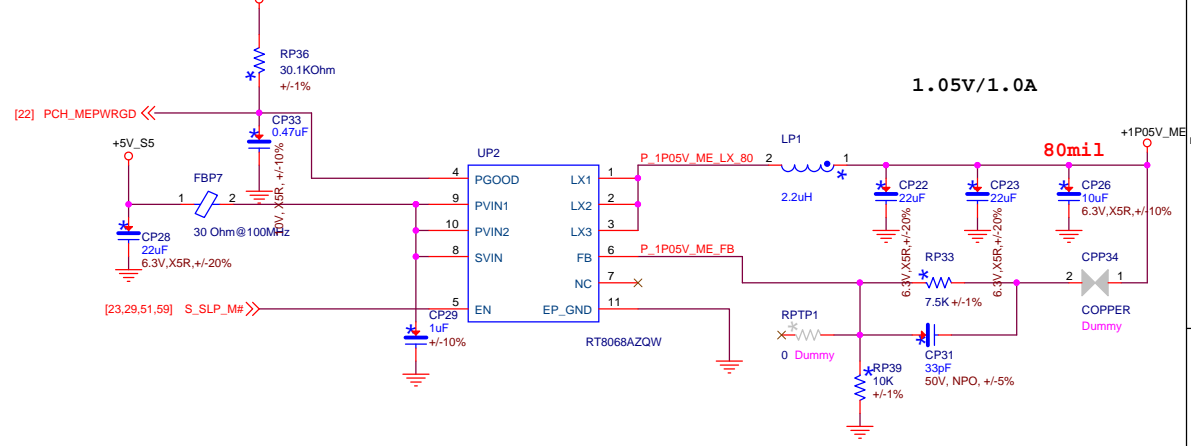
+V\_1.05\_PCH  
ENABLE CIRCUIT



+V\_1P5\_PCH



+V\_1.05\_ME

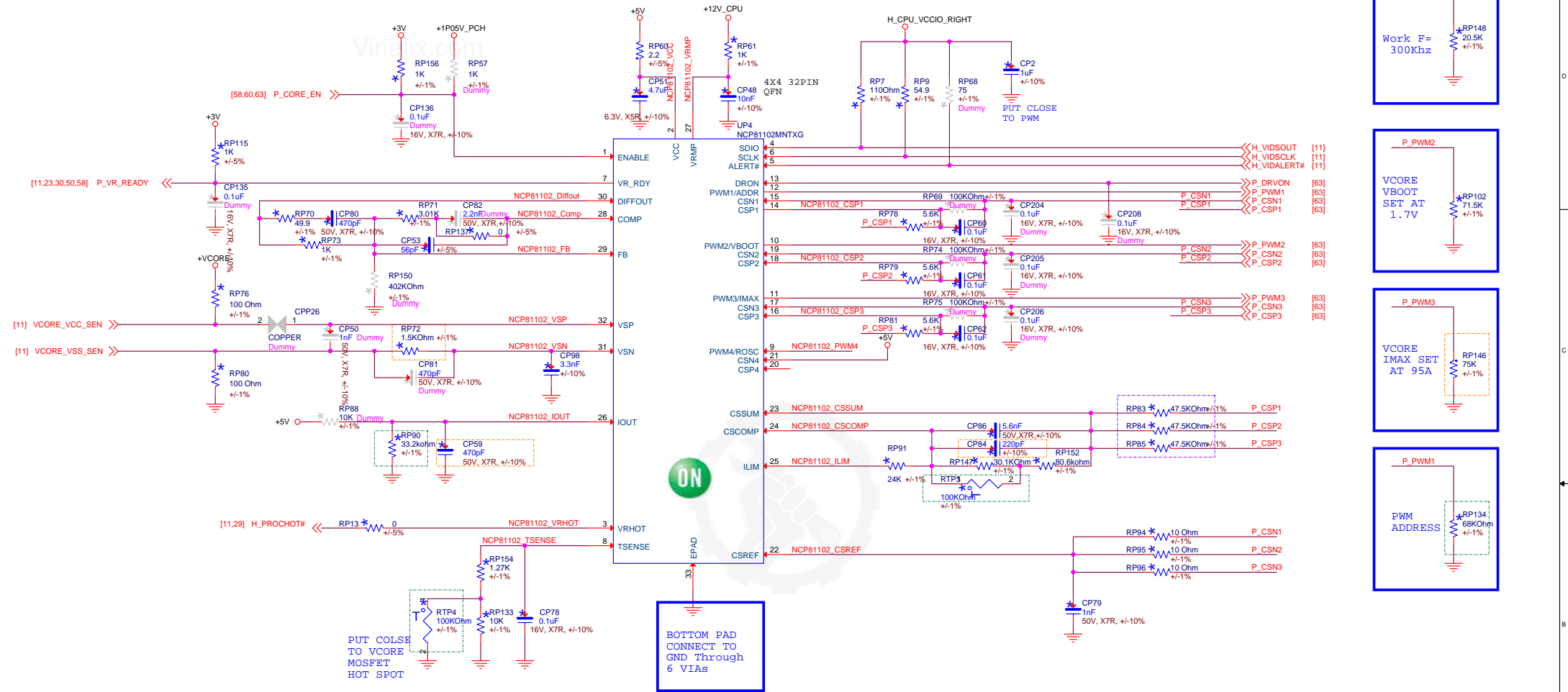


The schematic diagram illustrates the +5V\_DUAL\_USBKB power supply circuit. It is powered by +12VAUX and +5VSB. The circuit includes two AO3409L MOSFETs (QP101, QP102) and two AOD518 diodes (QP104, QP112). Key components include resistors RP712, RP717, RP720, RP721, RP722, RP735, RP733, RP292, and RP291, all with 1% tolerance. Capacitors include CP544, CP573, CP546, and CP572, with 10% tolerance. The circuit is controlled by DUAL\_POWER\_ENABLE and S\_SLP\_S4# signals. The output is +5V\_DUAL\_USBKB\_R and +5V\_DUAL\_USBKB\_F.

[illegible]

				INC.	
Title					
<b>Power-3:Linear Power-3</b>					
DWG NO				Rev	
<b><i>Tulum/Amazon MT</i></b>				<b>A00</b>	
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# SharkBay VR12.5 POWER CKT -3PHASE



Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.
10K	250Kh	30.9K	340Khz	61.9K	430Khz	105K	520 Khz	165K	610Khz
12K	260Kh	34K	350Khz	64.9K	440Khz	110K	530Khz	174K	620Khz
14K	270Kh	36.5K	360Khz	69.8K	450Khz	115K	540Khz	182K	630Khz
16.2K	280Kh	40.2K	370Khz	73.2K	460Khz	121K	550Khz	191K	640Khz
18.2K	290Kh	43.2K	380Khz	78.7K	470Khz	130K	560Khz	200K	650Khz
20.5K	300Kh	46.4K	390Khz	82.5K	480Khz	137K	570Khz		
23.2K	310Kh	49.9K	400Khz	88.7K	490Khz	143K	580Khz		
25.5K	320Kh	53.6K	410Khz	93.1K	500Khz	150 K	590Khz		
28K	330Kh	57.6K	420Khz	100K	510Khz	158 K	600Khz		

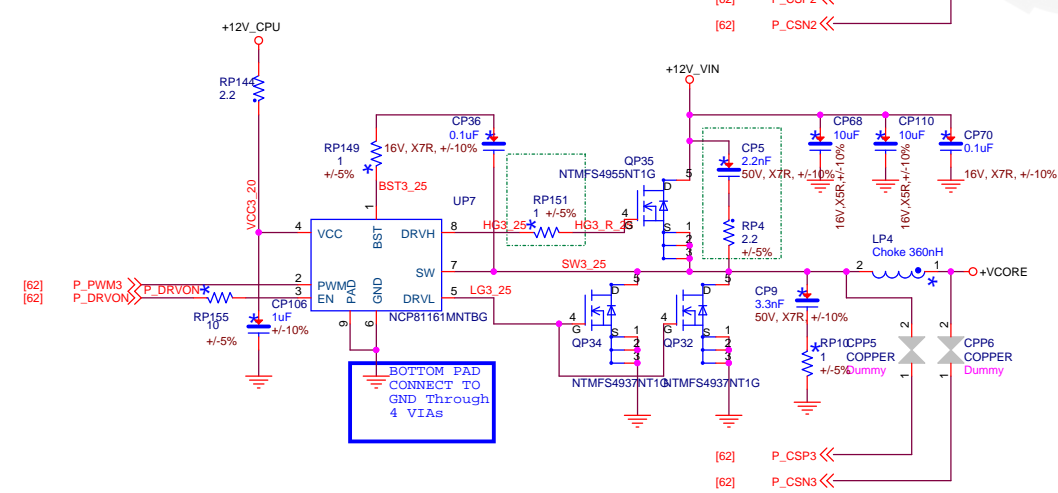
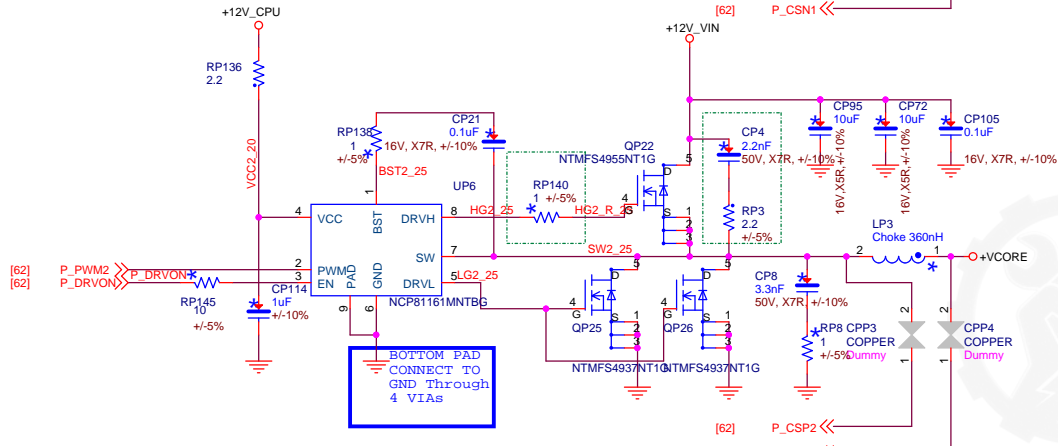
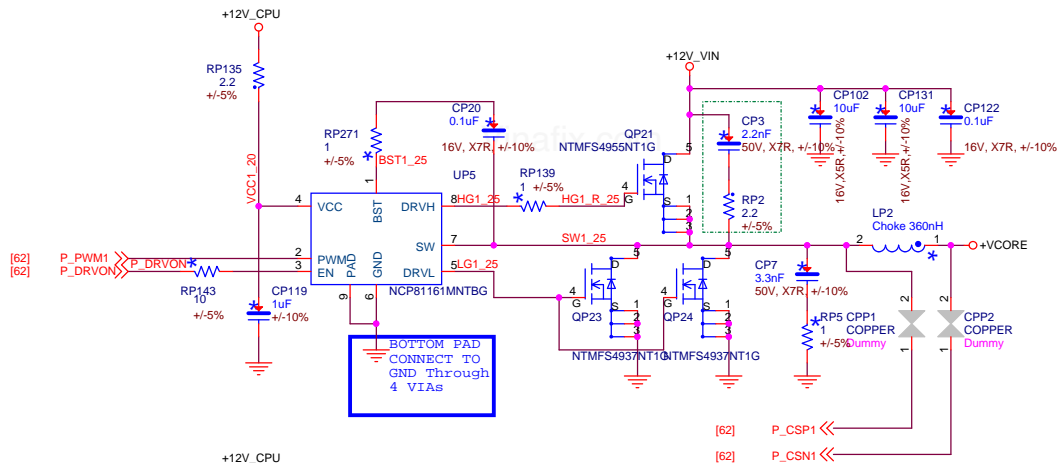
**INC.**

**Title**  
**Power-4:VCore**

**DWG NO**  
**Tulum/Amazon MT**

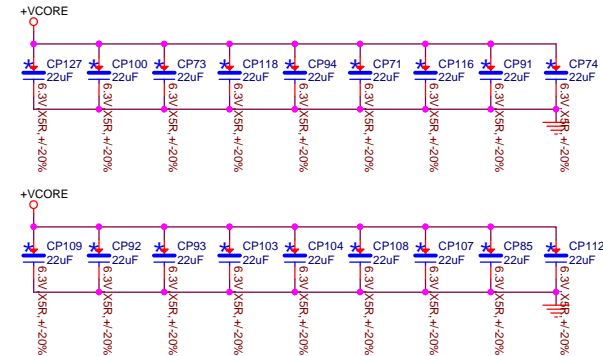
**Rev**  
**A00**

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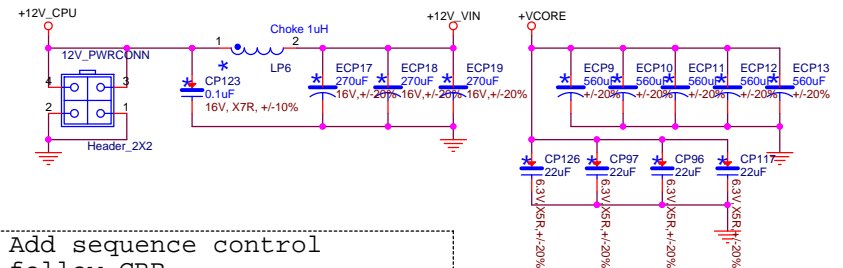
# CAD NOTE:

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY



# CAD NOTE:

PLACE CAPS AT TOP SOCKET EDGE



Add sequence control follow CRB

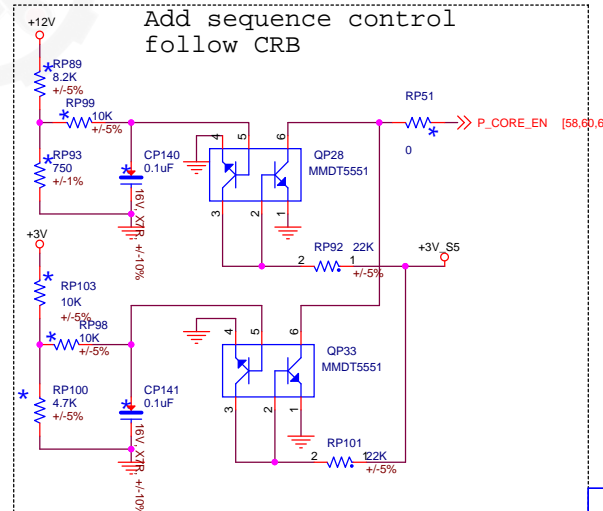




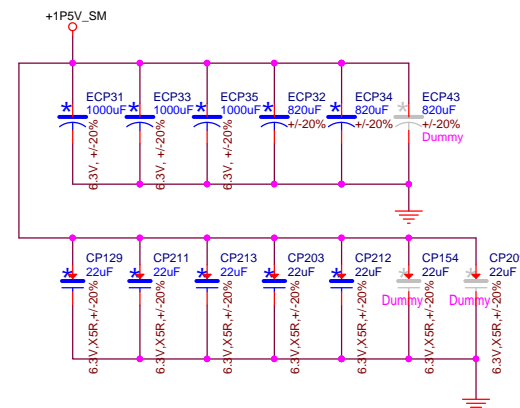
Diagram illustrating the circuit for the RT9045ZSP voltage regulator, showing the connection of the input, output, and feedback network.

**Components and Connections:**

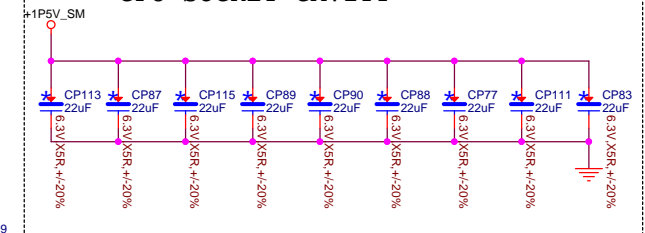
- Input:** +1P5V\_SM (1.5V) connected to VIN (Pin 1).
- Grounding:** GND\_1 (Pin 2) and GND\_2 (Pin 9) connected to ground.
- Feedback:** REFEN (Pin 3) connected to VTT\_REFEN.
- Output:** VOUT (Pin 4) connected to +5V.
- Capacitors:**
  - CP199 (10uF, 6.3V, X5R, +/-10%) connected between VIN and ground.
  - CP197 (1uF, +/-10%) connected between +5V and ground.
  - CP300 (10uF, 6.3V, X5R, +/-10%) connected between +1P5V\_SM\_VTT and ground.
  - CP198 (0.1uF, 16V, X7R, +/-10%) connected between the output of the feedback network and ground.
- Resistors:**
  - RP127 (1K, +/-1%) connected between +1P5V\_SM and VIN.
  - RP126 (1K, +/-1%) connected between the output of the feedback network and ground.

**Notes:**

- Bottom PAD CONNECT TO GND VIA 6 vias



PLACE ALL 0805 CAPS INSIDE  
CPU SOCKET CAVITY



### Power-6: DDR3

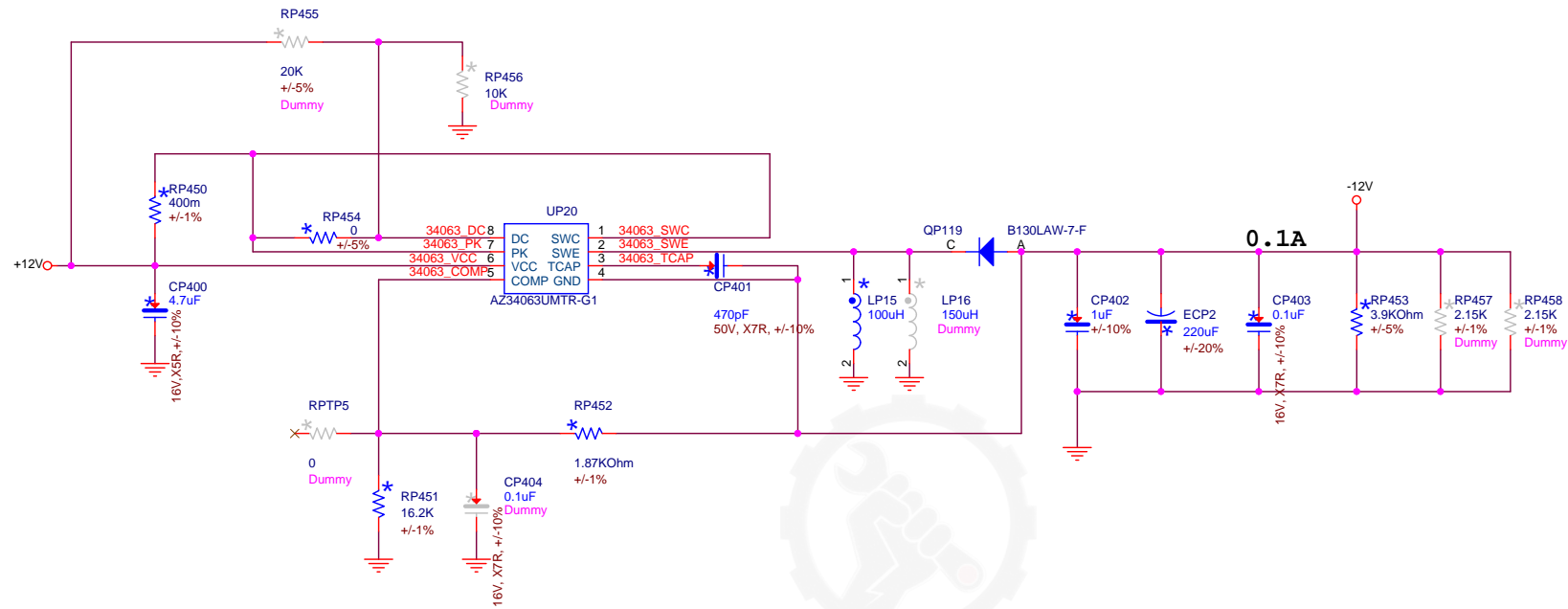
***Tulum/Amazon MT***

Rev	<b>A00</b>
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Vinafix.com



Title		
Power-8: -12V		
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